Challenges in Gate Level Modeling for Delay and SI at 65nm and Below

Jelena Frtunik
e-mail: jelena.frtunik@mytum.de

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Abstract

This report presents the concept of the gate level modeling. As we go further into the process of scaling the need of having more accurate and precise model of the cells is much greater. A resume of the existing cell models, as well as their strengths and weaknesses, is made in this paper. The paper is based on a presentation that was done during the Moscow Bavarian Joint Advanced Student School in March 2009.

Contents

1 Introduction

As processes move deeper in the nanoscale range, especially at 65nm (and below) CMOS technology node, silicon accurate performance modeling becomes very critical for IC designs. This is due to the fact that the absolute performance of CMOS transistors keep improving which leads to improvement of the chip performance. Taking this into consideration the chip performance metrics nowadays need to be measured with better absolute accuracy.

Metric that is used for measuring the performance of chip is the Statistical Timing Analysis (STA). In static timing analysis, we propagate the latest arrival time and transition time throughout a circuit and derive the longest/shortest path delays. Static Timing Analysis provides a key measurement for the circuit performance, which may as well be used for optimization purposes. Current trends in process scaling have imposed significant difficulties to STA which from 130nm usually also accounts for the effect of coupling between signal nets, or crosstalk.

During the development of any EDA system a great attention is payed in the implementation of an efficient and accurate STA capability. As we already know STA deals with path-tracing and becomes even more compute intensive with addition of coupling effects and variability computations. In addition, the accuracy requirements on STA have become more bounded with each new technology generation. The relation between the result of the STA analysis and the actual silicon is determined by the accuracy of the Delay Calculation (DC). DC can be considered as a circuit simulation that uses cell models. Taking this into consideration, in order to have more accurate results it is very important, the cell models to represent faithfully the behavior of the circuit. This leads to the fact that the cell models must be based on physical reality.

Most of the CPU time in STA analysis is spent in DC. Hence delay simulation needs to be very efficient, which depends on the efficiency of the models as well as the efficiency of the simulation algorithm. The STA flow is based on:

- cell models
- delay calculation
- graph algorithms

In this paper we will discuss the already known cell models as well as the challenges in cell modeling for STA. These provide abstractions of a standard cells circuit for a cell-level DC. In the delay calculation a simulation of a small subcircuit called stage consisting of driving and receiving gates and (coupled) interconnect parasitics is done.

As we know, in custom designs a transistor level delay calculation is used. Using a spice-like engine the simulation which is done is computationally very expensive. In comparison, a cell level DC employs an abstraction of the stages circuit built upon efficient cell models of drivers and receivers, as well as reduced-order models for interconnect. In both case, DC computes parameters (such as delay and slew) of the signal transition which are

relevant for timing analysis. These parameters are proceeded to the traversal algorithms, in order to determine the worst-case scenarios of design performance.

It is well known that CMOS circuits consist of CMOS gates and interconnects, and currently delay times of each part, i.e. the gate propagation delay and the interconnect propagation delay, are separately calculated. CMOS gates are non-linear devices and the estimation of gate delay is inherently complicated. Therefore, delay calculation based on look-up tables is widely used. This approach usually requires a prior characterization process to build look-up tables using a circuit simulator. Due to the limitation of circuit simulation costs, gate characterization is usually performed in two-dimensional space; output loading and transition time of input waveform (slope). The parameter of slope aims to capture the influence of waveform shape on gate delay. Recently many factors make transition waveforms more diverse in nano-meter technologies, such as crosstalk noise, interconnect inductance and resistive shielding, and hence capturing waveform shape by using a single parameter of slope is getting harder. Nevertheless, the number of parameters to express waveform shapes does not increase because of gate characterization costs.

DC is the core technology of STA and due to this fact the cell models used by a DC should be capable of satisfying the requirement in terms of features, accuracy, and efficiency. The main intent of this paper is to present the various gate modeling techniques and compare them in aspects of timing and noise analysis. Furthermore, the challenges with the existing and future cell models, their generation, storage and usage are discussed.

2 Cell Delay Models Taxonomy

When we speak about the cell delay model taxonomy we have to explain what exactly is modeled and how (on which way) it is modeled. The most important thing is that the cell models must accurately represent the behavior of the circuit.

As we have said earlier in order to determine the delay calculation we have to find the voltage transition of the stage. Nowadays each gate has to be considered with two different models because in a design we can say that a gate acts as a receiver in one stage and also as a driver in another stage. Historically the both of the roles were represented with just one single model which is not the case today.

In the following subsections the historical evolution of the driver models as well as the evolution of the receiver models is presented.

2.1 Driver Models

As we have mentioned before there are two different models for each gate. As far as the driver model is considered, the historical evolution of it is given in the following list:

- *Constant-delay model*: delay of each gate is defined independently of input slew and output load.
- *Load(fanout)dependent delay model*(single-parameter model): delay depends only on the capacitive load driven by the gate.
- *Input-slew/output-load delay-slew model (SLDSM)*(two-parameter model): output transition parameters (delay and slew) are defined as functions of output load and input slew.
- *Extended SLDSM, or ECSM*: same parameters as in SLDSM. In addition to the informations about delay and slew the model contains more detailed profile of the voltage response (transition).
- *Current-source model (CSM)*: defines drawn current as a nonlinear function of several parameters (input voltage and time, or input and output voltages).

The first four models can be categorized as Voltage-Response Models (VRM) because they define characteristics of the voltage response at the gate output as function of input slew and output load. The advantage of these models is that they determine the gates delay and output slew using simple look-up tables and interpolation.

Compared to the VRM models the Current Source Model (CSM) is represented with nonlinear voltage-controlled current source, which approximates the current drawn by gate for certain value of input voltage, time, output voltage. In order to determine the delay and slew, the CSM model has to perform circuit simulation which is not the case with the VRM models.

The major factor for transition from VRM to CSM is that the second can easily deal

with the complex (coupled) interconnects, crosstalk, IR-drop, Environment/process variations, Back-Miller effect etc. However, the usage of the CSM models is not at all cheap and simple because it requires changes in the library standard and the characterization methods.

2.1.1 Voltage Response Models - VRM

From all known VRM models, the Non-Linear Delay Model (NLDM) is the most widely used. In this model the two main parameters of a gate output transition, delay -D and output slew -T_{out} are functions of two input parameters: input slew - T_{in}, and output load - C_{load} and are defined like:

$$D = F_d(T_{in}, C_{load}) \tag{1}$$

$$T_{out} = F_s(T_{in}, C_{load}) \tag{2}$$

This definition of the delay and output slew works well just in the cases where:

- the interconnect parasitics can be represented by a single linear capacitor
- crosstalk is small
- details of a transition other than slew can be neglected

The functions that describe the delay and the slew are represented through 2-D tables. The determination of the D and T_{out} during the delay calculation is done by 2-D interpolation on the delay and slew tables. An important advantage of this model is that delay and slew values on the grid points are exact. However, in-between the grid point the success of determination of the D and T_{out} depends greatly on number of grid points and their values, as well as the interpolation method used. There are many interpolation techniques that can be used in the process of evaluation of the delay and slew (bi-linear, quadratic and cubic interpolation). They differ between each other because each of them provides different trade off options in terms of accuracy and computational cost. However, finding an efficient interpolation technique that gives physically correct values between the grid points and small errors is still a challenge.

Apart the problem that appears with the usage of the interpolation techniques, another problem arises when T_{in} or C_{load} are outside of the corresponding characterization range. In such cases a lower-order extrapolation technique can be used. This is very robust technique which does not completely eliminate the chances of getting a non-physical result.

In order to avoid the mentioned problems, Synopsys uses a polynomial representation of equations (1) and (2). This is done in the SPDM model, which might have less accuracy, due to fitting process but it has smaller evaluation time.

2.1.2 Current Source Models - CSMs

In this section we will discuss the different CSMs that have been proposed in the literature. The term Current Source Model denotes a family of cell models where each output pin is described using a nonlinear voltage-controlled current source. The differences between the various CSMs is in the way in which the current is represented and parameterized and as well as how it is used in DC for computing response.

Generally speaking, most of the CSMs for drivers have the following form:

$$I_{drv} = F_i(V_o(t), t, p_1, ..., p_N) \tag{3}$$

where :

- I_{drv} is the current that is drawn by the driver
- $V_o(t)$ is the voltage at the output of the gate
- t is the time
- p_i $(1 \leq i \leq N)$ stands for a parameter like V_{dd} or temperature.

The function F_i usually has a nonlinear algebraic or integro-differential form and contains the input voltage $V_i(t)$, time, and the voltage at the output pin of the gate.

In [AKM+06] the Multi-port Current Source Model, the function F_i is a function of voltages at all cells terminals. This model can handle simultaneous switching of multiple inputs. MCSM also has the ability to tackle a lot of other problems affecting timing analysis accuracy complex input waveforms, power-drop, signal integrity, delay variations due to cross capacitances, RC/RLC loading, etc. This model is described and discussed a little bit more in section 2.2.1.

However, as mentioned before the goal of DC is to determine the output voltage response. In order to do calculate that, the current given by equation (3), which is unknown in advance, is determined by numerical solution of the state-space system. This system describes the voltage responses on the nodes of a stage with the following formulae:

$$E\frac{dx}{dt} = Ax + Bu(V, t) \tag{4}$$

$$V = Cx \tag{5}$$

where:

- E, A are the capacitance and conductance matrices
- B, C are the port connectivity and observation matrices
- V is the vector of voltages at the terminals of the stage
- x is the vector of states

- $u(V,t)$ is a vector of current sources attached to the ports

In the current source models the current drawn by a cell having a single Channel-connected Component (CCC) can be accurately represented similarly to a source-drain current in a MOS transistor. Having this in mind, the current can be represented in this form:

$$I_{drv} = F_i(V_i, V_o) + G(\frac{dV_i}{dt}, \frac{dV_o}{dt}, V_i, V_o) \tag{6}$$

where V_i is a voltage on input of a CCC.

As we can see, the first term in the equation (6) is a function of the instantaneous values of V_i and V_o and it refers to the current source. Usually it is called a dc-current or static current because it is characterized using a dc-simulation.

The second term represents the dynamic current which comes from the nonlinear capacitors of the cells transistors and can be linearized with respect to the time-derivatives $\frac{dV_i}{dt}, \frac{dV_o}{dt}$ which leads to:

$$G = c_m(V_i, V_o)\frac{dV_i}{dt} + c_g(V_i, V_o)\frac{dV_o}{dt} \tag{7}$$

where:

- c_m corresponds to Miller capacitance
- c_g corresponds to the output capacitance

One well known CSM model is the Blade model [CW03]. As shown in Fig. 1 it consists of a voltage controlled current source, an internal capacitance ($C_{internal}$) and time shift of the output waveform. This model represents the electrical performance from an input pin to an output pin under the conditions from which the current source was derived. Derivation of a Blade model is accomplished in two steps. The first step is to determine the amount of current sourced by a cell in response to voltage levels on the input and output pins of interest, $i_{out}(V_{in}, V_{out})$. Specifically, for a given process corner, voltage, and temperature, a delay calculation voltage supply is attached to the input pin of interest and another to the output pin of interest. The two voltage sources are then swept from V_{ss} to V_{dd} and the current sourced by the cell's output pin is measured to create an I-V table. Furthermore, this table is used to determine the cell's transient response from which the delay and the slew can be calculated.

Accompany to the Blade model is a Razor model which represents the interconnect. This interconnect model can handle the arbitrarily complex voltage waveform created by the Blade model and accurately calculates the resulting waveform used to drive the next Blade model, all at speeds 5-6 orders of magnitude faster than SPICE.

The Blade and Razor model has a high performance, accurate runtime and properly handles dynamic effects of noisy and elongated input waveforms.

It is important to mention that with the equation (6) we can only model a single CCC cell. However, in case of multi-CCC gates like AND, OR etc. it fails to provide adequate accuracy. The main reason lies in the fact that the output current is not a

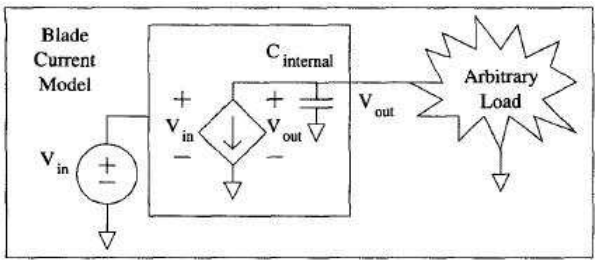

Figure 1: Blade model [CW03]

function of instantaneous input voltage, but rather of some other transition, which we label as $w(t)$. In many cases $w(t)$ represents the fact that the input voltage has been shifted in time, distorted and possibly inverted compared to the original V_i, and may have complex (integro-differential) relation to it. Usually, for most simple multi-CCC gates, $w(t)$ is a transition at the input of the last CCC. This transformation of the input voltage in the case of multi-CCC gate mathematically can be expressed with:

$$I_{drv} = F_i(w, V_o) + G(\frac{dw}{dt}, \frac{dV_o}{dt}, w, V_o) \tag{8}$$

where $w(t)$ can be found from:

$$w(t) = J(V_i) \tag{9}$$

A we can see from the equation above the operator J represents the transformation of the input voltage $V_i(t)$. During the past years several different approaches in order to represent the function J have been proposed.

In [KTV04] the operator J is based on a lookup table representing the slew of $w(t)$ as a function of slew of V_i. This methodology, which is robust and less pessimistic, can calculate the effect from the crosstalk on noise-on-delay analysis. The mentioned approach has been successfully used in the industrial tool CeltIC. The accuracy of the current model matches transistor level Spice simulations to within 2-4 percent.

In another model [CW03], each CCC is modeled in topological order using the equations (6) and (7). After that, several integrations of the state-space system (equations (4) and (5))are preformed in order to find $w(t)$. This is very costly approach and works only for simple types of models. This is due to the prevalent nonlinear capacitance of the internal nodes of multi-CCC cells. As consequence of this fact it is not so clear how accurate this method is.

Furthermore, J can be represented with a linear passive circuit, with fitting the parameters to match the time shift and distortion of $w(t)$ relative to $V_i(t)$ [LFA07]. The disadvantage of this method is that it is not so clear how well this method works for different types of cell (especially for the ones that have multiple strongly nonlinear CCCs).

In the above mentioned models a partitioning of the cells circuit into CCCs and characterizing each CCC with a dc-current table is done. This leads to the fact that we have to know and understand the internal topology of the cell. In order to overcome this disadvantage a new technique of constructing a multi-CCC CSM is described in [LFA07]. There we

have a piece-wise polynomial macro-model for the cells circuits [TR06]. Furthermore, this technique can handle complex input transitions, multiple-input switching and crosstalk.

2.2 Receiver Models

As mentioned before each gate in a circuit is be represented with driver model and receiver model. In this section we will describe the receiver model which is consisted of two parts. The first part is the Load Model (LM) which represent the impact of the receiving gate on the driving stage. Of great importance is also the second part called delay metric.

The Load Model can be described in two ways that are actually equivalent. One way to describe the impact of the receiving gate is in terms of current that is injected into the driving and the other way is by time-dependent capacitive load. The reason why both ways are the same lays in the formula $I = C\frac{dV}{dt}$.

2.2.1 Load Model

As said before one of the parts of the receiver model is the load model. The traditional load model is based on single capacitance value. Because of the stronger non-linearity of the capacitance in the recent process nodes there was evolution of the traditional load model. In the first model there were just two values (one for rise and one fall). Afterward a capacitance range was used to model the min and max delays. This model was followed by the model in which the capacitance was a function of input slew and/or output load. In the fourth model there was voltage-dependent capacitance and nowadays we have the CSM-based load model.

There are many CSM based load models and from my point of view the Multi-port Current Source Model appears to be more accurate than the others. It is also able to deal with the strong non-liner pin capacitance and the Back-Miler effect. A detailed modeling of the pin capacitance is very important especially in the cases where the load capacitance is dominated by the non-linear pin capacitance of the receivers.

The Multi-port Current Source Model (MCSM) consists of a nonlinear resistor in parallel with a nonlinear capacitor at each input and output pin (or port) of the cell. The resistor is represented by a voltage-controlled current source i_R and the capacitor by a voltage-controlled charge Q_C as shown in Figure 2. Because of the fact that each port in a nonlinear cell can behave differently, it is reasonable to expect that the voltage-dependent values of i_R and Q_C at each port are different. These values are given by [AKM$^+$06] :

$$i_{R,p_i} = f_i(V_{p1}, V_{p2}, ..., V_{pn})$$

$$Q_{C,p_i} = g_i(V_{p1}, V_{p2}, ..., V_{pn})$$

where f_i and g_i are precharacterized functions (stored as tables or equations) of port voltages V_{p_i}. For example, the MCSM model for a two input NAND gate will consist of three ports: one for each input and output.

Despite the fact that this model deals very well with the Miller effect it is not practical

to use on large scale design because it requires modeling of all receiver nodes as ports. Furthermore, the computation of response becomes costly because it requires simulation of a state-space model with multiple current sources.

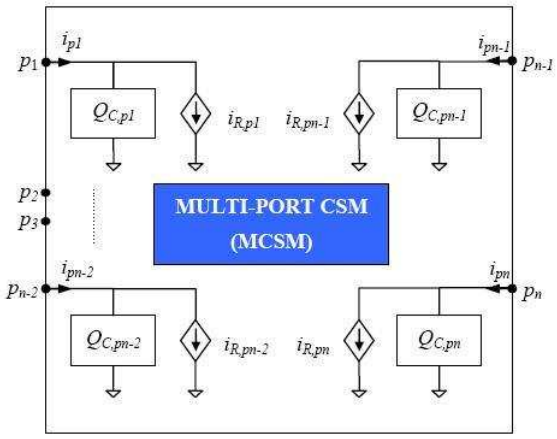

Figure 2: Multi-port current source model[AKM+06]

2.2.2 Delay Metric - DM

Delay metric is the second part of the receiver model and its functions is to represent the voltage response in terms of some important characteristics such as delay and slew. Earlier the delay and the slew were determined from the voltage response waveform by finding the V_{ref} for the delay and V_L, V_H for the slew. In addition, in the past the libraries defined uniform threshold among all library cells, directions and arcs which is not the case today. Nowadays the libraries contain pin dependent thresholds.

As we have mentioned several times in the paper due to the scaling process there are many factors (crosstalk, resistive shielding, wire inductance) that have to be taken into consideration when we calculate the delay. There are several new timing analysis scheme that have taken those factors into account and one of the most important is the equivalent waveform model or EWM.

The EWM scheme does not calculate the latest arrival time and the slope from the timings when the waveform goes across reference voltages. What it actually does is that it derives an equivalent input waveform with a standard shape such that the equivalent input waveform produces an output that matches with the actual output waveform. In equivalent waveform calculation we have to find out which part of the input waveform dominantly determines the output transition. After determining the metric that points out the important waveform region, an equivalent waveform calculation method based on the least square fitting with the devised metric is developed. This method does not change other parts of delay calculation i.e. no library extension and no additional gate characterization are necessary. Hence EWM is easy to work with conventional STA methods.[HYO03]

3 Library Characterization

As mentioned many times before at 65nm and below, we must already consider crosstalk and variability effects which lead to a change of the gate level models. Furthermore, this lead to a change in the library and they tend to be more complex, take more storage and runtime. In order to produce a high accuracy standard cell library, the library characterizer has to perform millions of transistor-level simulations which usually takes some days. With the number of process/environment parameters potentially reaching tens, the characterization run time and size of variation aware extensions of the standard-cell libraries grows significantly which leads to usage of gigabytes of disk space. In order to overcome these problems the industry uses parallel computing and more compact storage of the models like the binary format.

A typical library characterization flow is consisted of the following 4 major steps:

1. sensitization of input vectors
2. setting up and performing circuit simulations
3. collecting and processing results
4. generating libraries

In the following three subsection a detailed description of the characterization algorithm for the driver and the receiver model is given.

3.1 Driver Model

The characterization process of the driver model differs depending on whether the gate is represented by VRM or CSM model. The procedure which is used to characterize the Voltage Response Model is relatively simple and it is consisted of the following steps:

1. Given an input slew and an output load, a transistor level simulation is performed by applying a voltage source at the input and a lumped capacitive load at the output.
2. The slew and the delay in the case of NLDM are measured from the simulated voltage waveform.
3. The process is repeated for a list of predefined input slews and output loads leading to several 2-D tables.

There are some drawbacks in terms of accuracy when we speak about the VRM characterization. Hence, it is not so clear how to choose values on input slew and output load in order to minimize the interpolation errors in DC. Furthermore, the measurement of slew and delay on the output transition involves interpolation between time points that are chosen internally during the SPICE simulations, which can produce an error.

The Composite Current Source (CCS from Synopsis) modeling technology is the first

in the industry that proposed a complete open-source current based modeling solution for timing (composed of driver and receiver model) noise and power. Synopsys CCS is similar in terms of characterization flow to the VRMs. Instead of measuring and storing voltage waveforms WFs, CCS measures and stores current WFs consisting of time-current pairs along the transition. Usually the shape of the current that we get has a sharp profile and there is a need to store more time-current pairs in order to have high accuracy. This leads to larger disk size of the library which appears to be disadvantage in this model.

In comparison to the VRM, the CSM models are easier and faster to characterize. This is due to the fact that they require usage of less DC simulations which are cheaper than transient simulations required for VRM models. Furthermore, CSM models use less disk space because they are based on a voltage-controlled current sources which are independent of the parameters like input slew and output load. Albeit, an additional runtime cost of waveform processing is necessary because the measured current is likely to be much noisier than voltage waveforms.

3.2 Receiver Model

There are many ways in which the cell characterization of the receiver model RM can be done. Actually, a characterization of the load model is made here. The simplest method is based on adding the average gate and diffusion capacitances of the devices connected to the cells input pin.

Another way is by measuring the current through a saturated ramp voltage source attached to the cells input pin. With averaging over time (integration) we can determine the pin capacitance value. This method is more expensive but more accurate.

A third way to model the receiver is by measuring the the delay over the characterized gate driving three to four identical gates. This method uses load matching which means that in another simulation the same gate drives a capacitive load C_{in}, which is iteratively changed until the delay observed matches with that from the circuit with real gates as loads.

3.3 Extension to Process/Environment Variations

Nowadays, variation-aware STA, either multi-corner or statistical STA, requires specially constructed libraries providing way of computing, respectively, delays for different corners and sensitivity of delay and slew with respect of process and environmental parameters.

The multi-corner STA requires multiple standard-cell timing libraries, generated using different process, voltage and temperature (PVT) parameters in the transistor level simulations. We can say that in the multi-corner STA the computational effort is proportional to the number of required libraries. In order to reduce (shorten) the characterization time the parallel computing can be implemented. Beside this fact, there are still some problems like:

- The input vector sensitization step is common for different corners.

- The selection of characterization corners, can be different from that desired by variation aware STA users. Due to this a multi-dimension interpolation of the models is required, which can lead to numerical errors.
- Multiple libraries are usually kept in different files (single file is desirable).

As for the case of SSTA, we already know that in this method the timing, power, and signal integrity characteristics of each element in the device are represented with Probability Distribution Functions (PDFs). In order to characterize the cell models in an SSTA flow the cell model should provide sensitivity of voltage WFs (including delay and slew) for VRMs, and current for CSM with respect to number of process and environmental parameters. One way of getting the sensitivity data is by implementing the following method which is consisted from three steps:

1. A full set of simulations for characterizing the library is performed with a small change of the process parameter.
2. The resulting measurement is used to compute the sensitivities.
3. The previous steps are repeated for each process parameter. A set of linear equations for sensitivity is formulated and solved in transistor-level simulator. The set is derived from the original circuit equations by linearizing them around the nominal set of process/environment parameters and responses.

Compared to the previous method there is another method that is more efficient and accurate. This method uses a set of linear equations for sensitivity which are formulated and solved in transistor-level simulator. After that, by linearizing the equations around the nominal points of process/environment parameters and responses we can find out the set.

4 Signal Integrity

In its most general sense, Signal Integrity (SI) means ensuring that signals faithfully propagate to their intended destinations within their allocated time frames. In the earlier technology nodes of 180nm and above, SI effects were typically analyzed and repaired manually after timing closure. This approach simply does not work with todays 90nm and 65nm technologies, because the number of potential violations of the design have increased dramatically. Reduced feature sizes, decrease in interconnect pitch, lower power supplies, the use of multiple power supplies, and the use of transistors with different switching threshold V_t voltages all contribute to SI-induced timing problems.

Todays low-power designs typically use multiple supply voltages, and coupling from a higher voltage signal to a lower voltage signal is significantly more severe than coupling between signals of the same voltage. Low-power designs also use gates formed from transistors with different switching threshold V_t voltages. Higher V_t devices generally have a higher holding resistance, which makes them more vulnerable as victims of crosstalk. By comparison, lower V_t devices have faster transition times, which make them more aggressive as attackers.

Another SI-related timing issue is when crosstalk effects cause setup or hold violations. Depending on whether signals are switching in the same or opposing directions, a transition on the aggressor may speed up or slow down the victim signal.

All these problems should be taken into account in the gate level models and the timing analyzer should report the potential violations accordingly.

5 Conclusion

Modeling requirements for accurate analysis of nanometer designs are growing faster than the ability to create models using the traditional characterization process. Considerations that need to be included in the design of the cell models at 65nm and below are the noisy and elongated input waveforms, crosstalk, nonlinear pin capacitance and Back-Miller effect.

Anyway, in the past years VRM models have been replaced by the CSMs. The reason of this transition is the fact that the Current Source Models can easily model the above mentioned phenomena. However, CSM models are more complex but much more accurate compared to the VRM models. Furthermore, today CSM models appear to be robust enough to survive next technology generations.

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