Characterizing Multistage Nonlinear Drivers and Variability for accurate Timing and Noise Analysis

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Design methods for micro- and nanoelectronic ICs and systems

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1. Introduction

1.1 Cause of Variations of Circuit Timing

- Imperfect CMOS manufacturing process
- Environmental factors such as drops in V_{dd}
- Substrate temperature changes
- Device fatigue phenomena
  - Electron-migration
  - Hot electron effects
  - Negative bias temperature instability

1. Introduction

1.2 Why is there an increasing deviation?

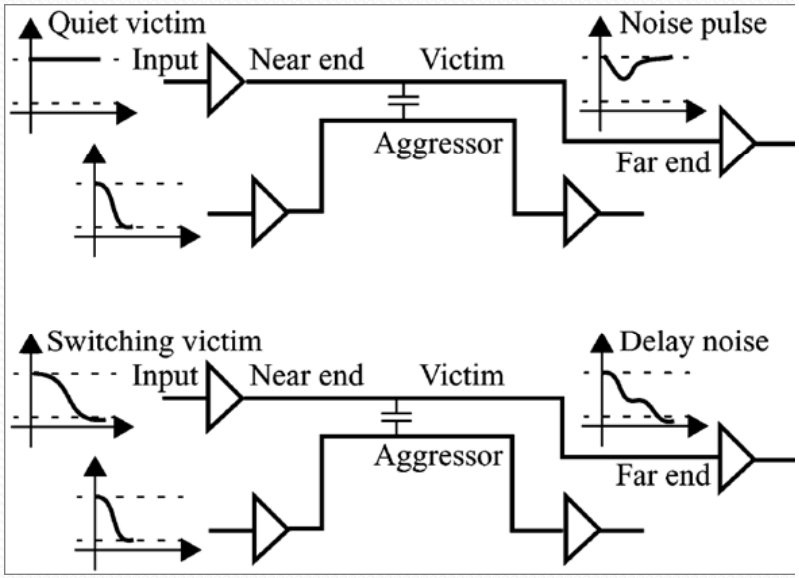
- Increasing circuit speed
- Crosstalk noise (smaller design process)
- Inductive coupling in nanoscale designs
- The impedance of the interconnect lines does not scale down by the same factor as the gate impedance

Deviations form the truth signal for the new designs ➔ new model necessary

1. Introduction

1.3 The two Types of Noise

- Functional noise
  - Noise induced in quiet nets → victims
  - Switching neighbors → aggressors



➔Can cause unwanted logic activity

- Delay noise
  - Caused by switching activity
  - Victim and aggressor are switching

➔Modify time of flight and slew-rate

1. Introduction

1.4 Criteria of a Good Model

- Adequate coverage for wave shapes typically seen in circuits
- Concurrent usage of both „old“ and „new“ model
- Intuitive parameters
- Simple gate characterization

  ➔no additional characterization necessary
- Minimal storage space for gate characterization
- Controllability of the complexity by the user

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2. The Different Models

2.1 Model Categories

1. Linear timing models

   C-effective technique ->system of nonlinear equations

2. Best-fit resistance models

   Based on the equivalent gate resistance and a transient holding resistive model -> reaction of the logic block modeled by a fitted resistance

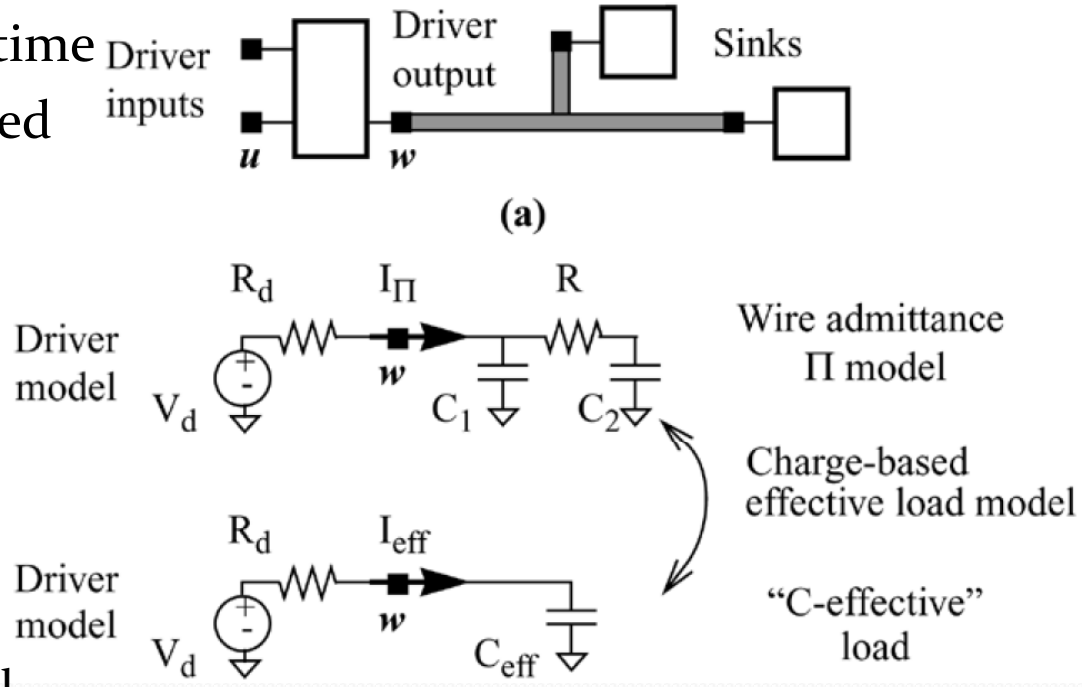
3. Large signal driver current models

   Derived using DC gate output current measurements

2. The Different Models

2.2 The most Popular Approach

- Characterizing the Waveform with a delay and a transition time
- Driving Admittance is modeled as a π-circuit
- Transformation to effective load



So we get:

- Very fast model
- Does deviate form the truth signal for the new nanoscale designs

2. The Different Models

2.3 The Variation-Aware Gate Timing Analysis

- Variation-Aware Gate Timing Analysis
  - here the RC-π load can vary by using canonical first order model (CFO)

$$A = a_{nom} + \sum_{i=1}^{m} a_i \Delta X_i + a_{m+1} \Delta S_a$$

$$= a_{nom} \left(1 + \sum_{i=1}^{m} \frac{a_i}{a_{nom}} \Delta X_i + \frac{a_{m+1}}{a_{nom}} \Delta S_a \right)$$

ΔX_i: variation of m global sources of variation

ΔS_a: random sources of variation S_a

  - imperfect CMOS manufacturing processes are considered

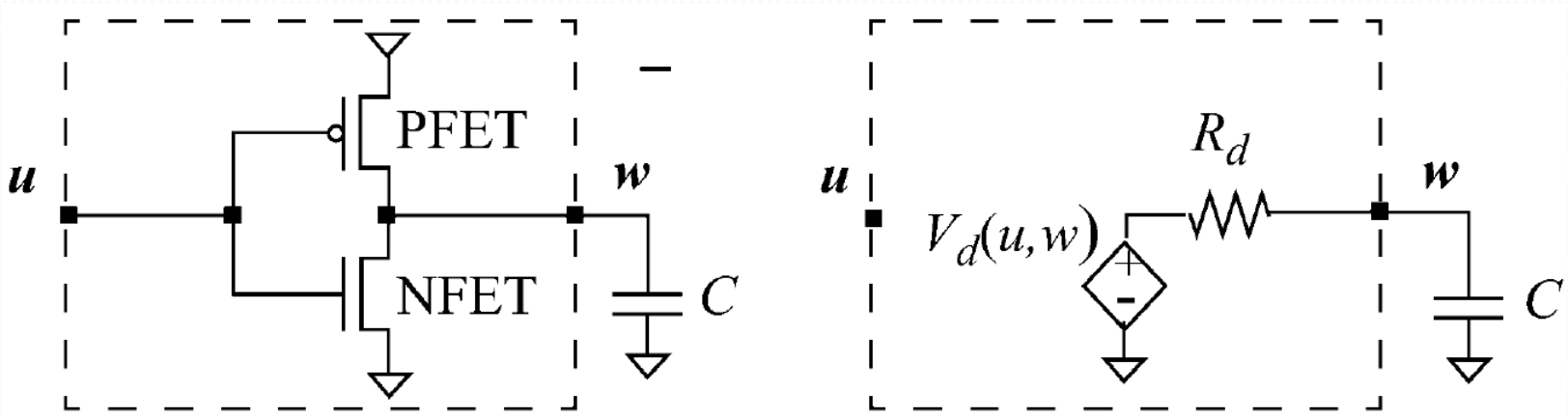
➔ Statistical timing analysis provides effective solution

- ➔ Average error of only 7%
- ➔ Runtime 145 times faster as spice

2. The Different Models

2.4 Model based on Finite Elements Method (FEM)

- Modeling of a nonlinear voltage source by FEM



➔Generates reusable models

➔Also delay noise can be modeled

➔Accurate within 1% for delays and 1.5% for rise times

2. The Different Models

2.5 Equivalent Waveform Propagation

- Capture of input waveforms for static timing analysis (STA)
- Derives an equivalent input waveform that produces the matching output waveform

$$\frac{\partial v_{\text{out}}}{\partial v_{\text{in}}} = \frac{\partial v_{\text{out}}}{\partial t} \cdot \frac{\partial t}{\partial v_{\text{in}}} = \frac{\partial v_{\text{out}}}{\partial t} \cdot \frac{1}{\frac{\partial v_{\text{in}}}{\partial t}}$$

➔ Minimize:

$$\int_{t_1}^{t_2} \left| \frac{\partial v_{\text{out}}}{\partial v_{\text{in}}} \right| \{f(t) - g(t)\}^2 \, dt$$

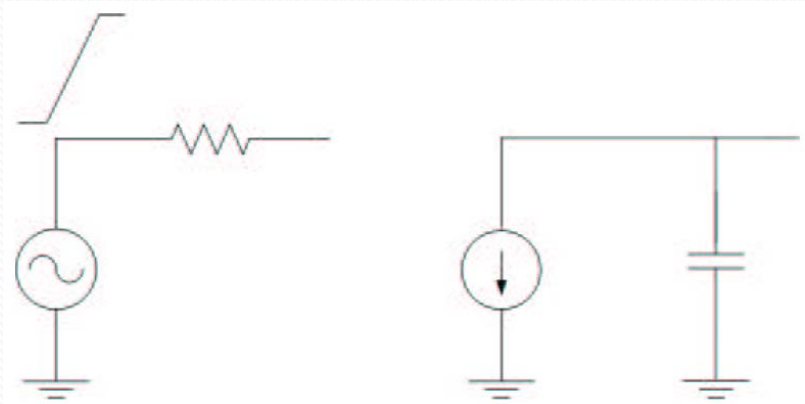
f(t): Equivalent waveform
g(t): actual waveform

➔ Easily implemented with conventional STA Tools
➔ Add-on to conventional tools
➔ More accurate timing with 15-30% more costs

2. The Different Models

2.6 Current-Based Gate Models

- Current-based gate model without further pre-characterization



➔ Includes power supply voltage drop

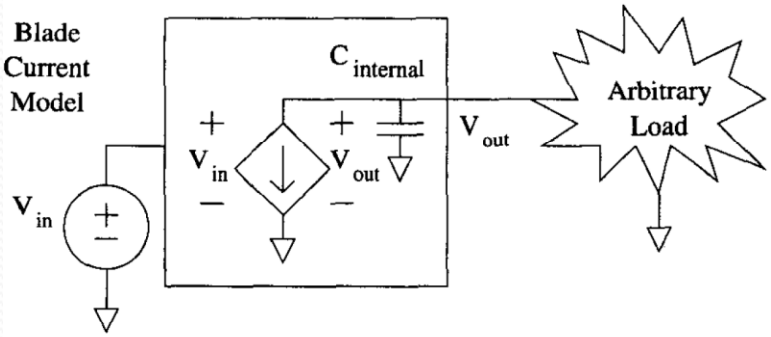
➔ Accuracy of up to 4.6%

(less accurate than pre-characterized models)

2. The Different Models

2.7 Blade and Razor

- Blade →novel cell model and runtime engine based on current flow



Voltage controlled current source

internal capacitance

time shift of the output waveform

- Razor → interconnect model
  - Novel implementation of recursive convolution

→ Tenth of thousands of times faster than SPICE

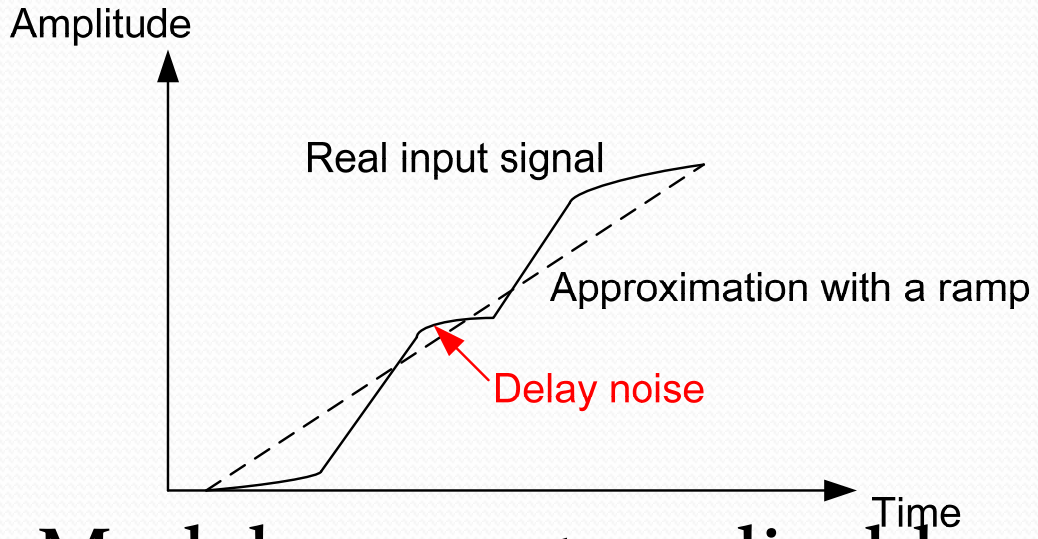
→ Operates on arbitrary input waveforms

2. The Different Models

2.7 Their problems

- These models are all only applicable for ramp signals
- No multistage modeling possible

Example:



- So our Models are not applicable any more!!

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    2. The Advantage of this aproach
    3. The Structure of the WiM
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4. Parametrizable Waveform Independent Model
5. Experimental Results
6. Conclusion

3. Waveform independent Model (WiM)

3.1 What is the difference?

- Model depends only on parameters out of Spice simulation (capture of circuit nonlinearities)
- Not waveform-centric approach
  - The idea is not to rebuild the waveform behavior

➔ Differs from the common practice where the gate is pre-characterized for a given (ramp) input

3. Waveform independent Model (WiM)

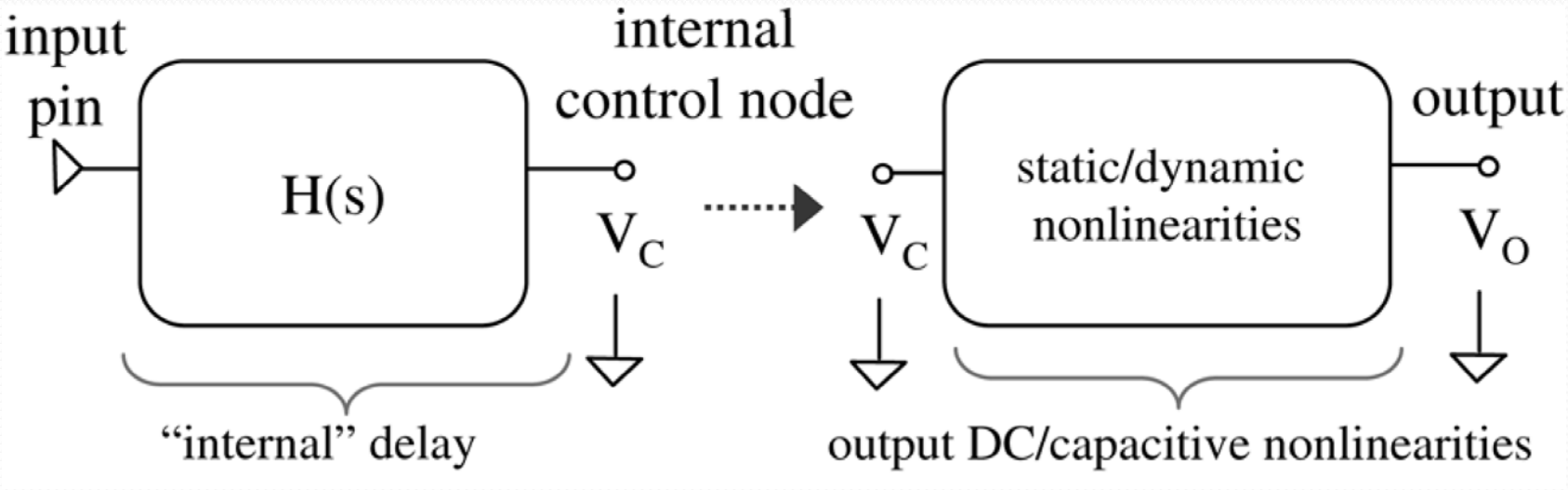
3.2 The Advantage of this approach

- Encapsulation of the intrinsic nonlinear dc and dynamic behaviors of a nonlinear driver
- Possibly of multistage
- Cost comparable to that of a waveform-centric model
- Can be applied to arbitrary input signals
- Suitable for capturing resistive shielding, inductive ringing, and capacitive and inductive coupling noise
- Accurate timing and noise analysis under process voltage temperature analysis
- Near Spice accuracy

➔ Reduction of the analysis runtime by 40%

3. Waveform independent Model (WiM)
3.3 The Structure of the WiM

- Internal control node → fictitious
- Internal Delay → linear dynamic input stage
- the static/dynamic nonlinearities → combined circuit nonlinear characteristics



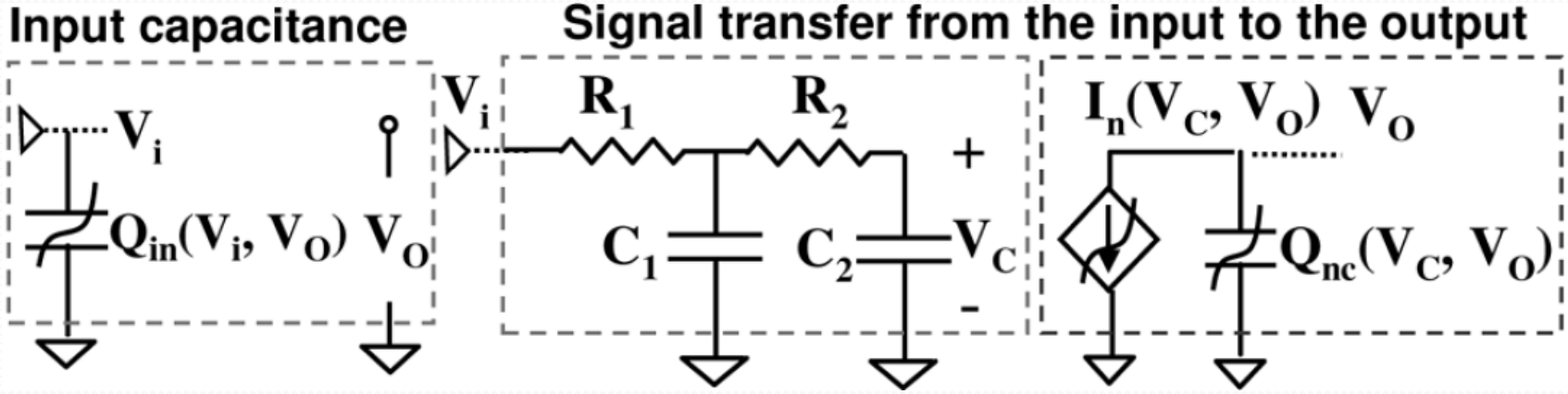
➔Possibility for multistage

3. Waveform independent Model (WiM)

3.3 The Structure of the WiM

1. Input capacitance models the loading to the preceding stage and is controlled by input and output voltage

2. The Transfer stage
   1. Second order linear RC-stage
   2. Nonlinear current source + Nonlinear Capacitance

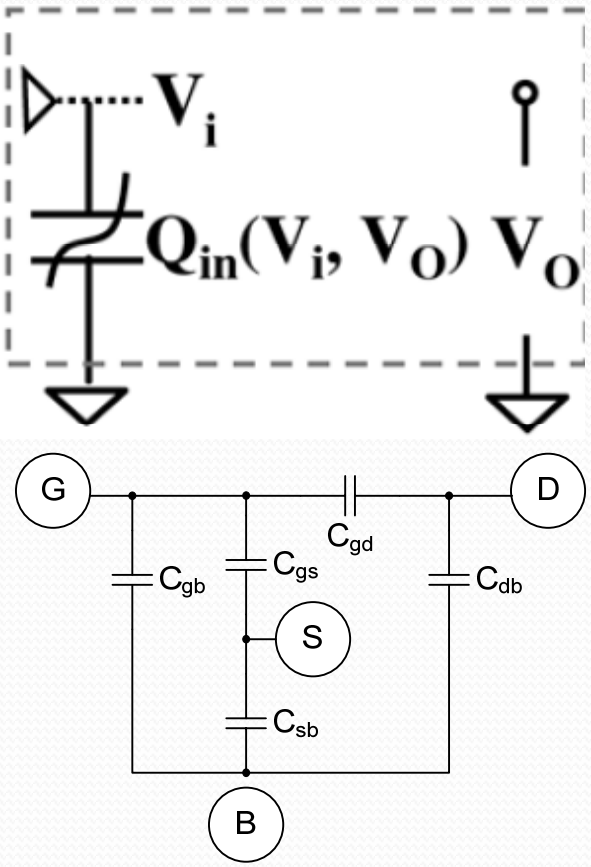


3. Waveform independent Model (WiM)

3.3 The Structure of the WiM

Input capacitance:

- depends on V_{input} and V_{output}
- simulates load to the preceding stage



Cutoff:

$$C_{gs} = w \cdot L \cdot C_{ox}$$
$$C_{gd} = w \cdot L \cdot C_{ox}$$
$$C_{gb} = w \cdot L \cdot C_{ox}$$

Saturation:

$$C_{gs} = \frac{2}{3} w \cdot L \cdot C_{ox}$$
$$C_{gd} = w \cdot L \cdot C_{ox}$$

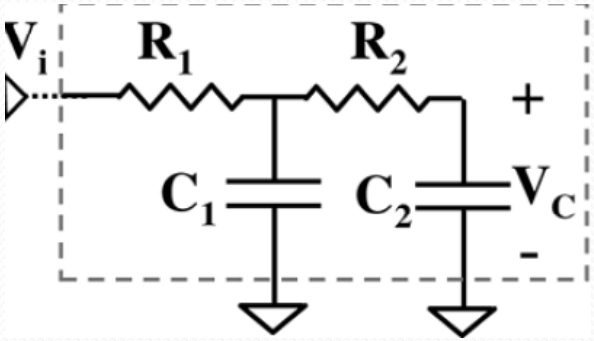
3. Waveform independent Model (WiM)

3.3 The Structure of the WiM

Transfer stage:

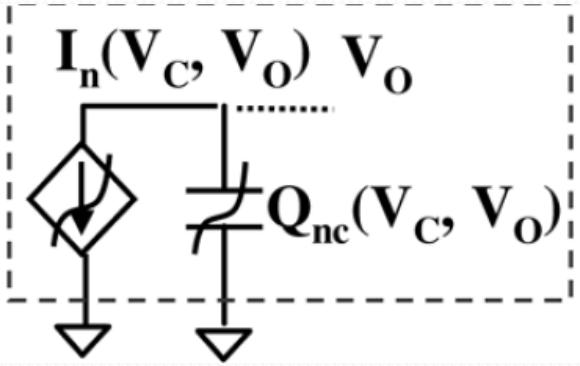
RC-Input Stage: second order model

- models wire



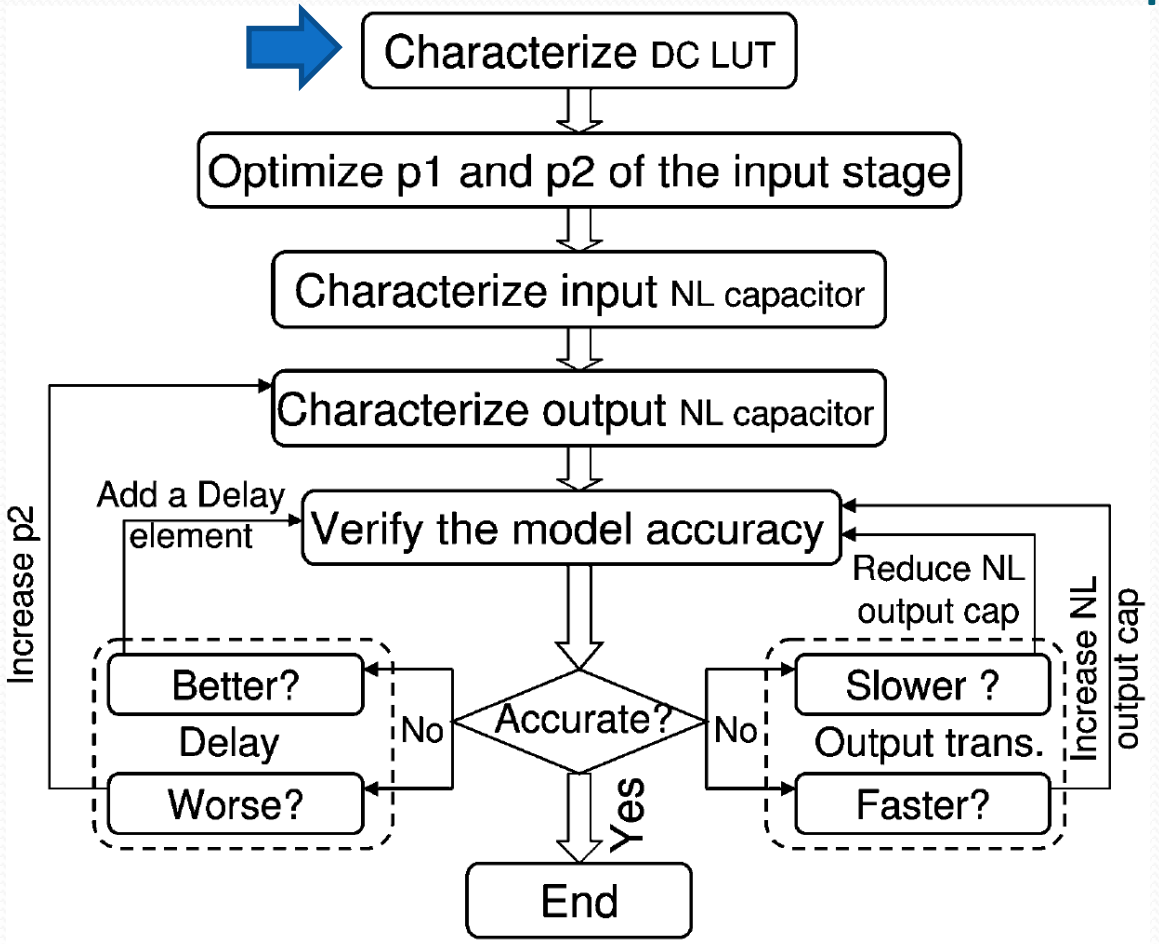
Nonlinear Output:

- $I_n(V_c,V_o)$ → models MOSFET behavior
- $Q_{nc}(V_c,V_o)$ → nonlinear charge voltage



3. Waveform independent Model (WiM)

3.3 Detailed Model extraction Steps

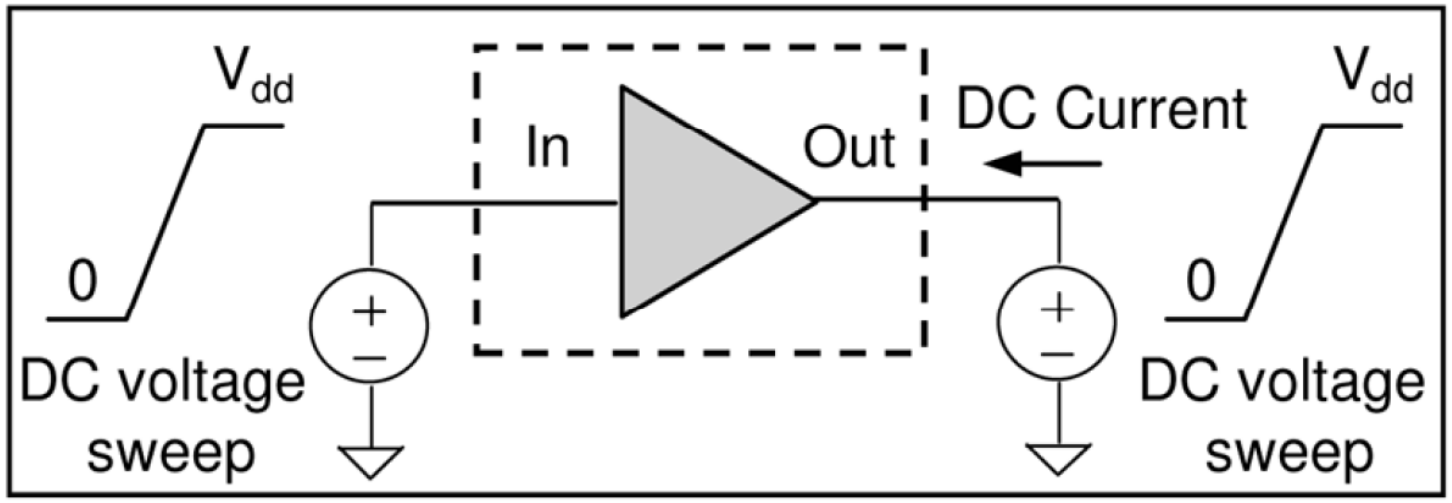


3. Waveform independent Model (WiM)

3.4 Detailed Model extraction Steps

Creation of the DC Current Look-up Table (LUT)

- Multiple DC-analysis in SPICE while sweeping the input/output current from o to V_{dd}



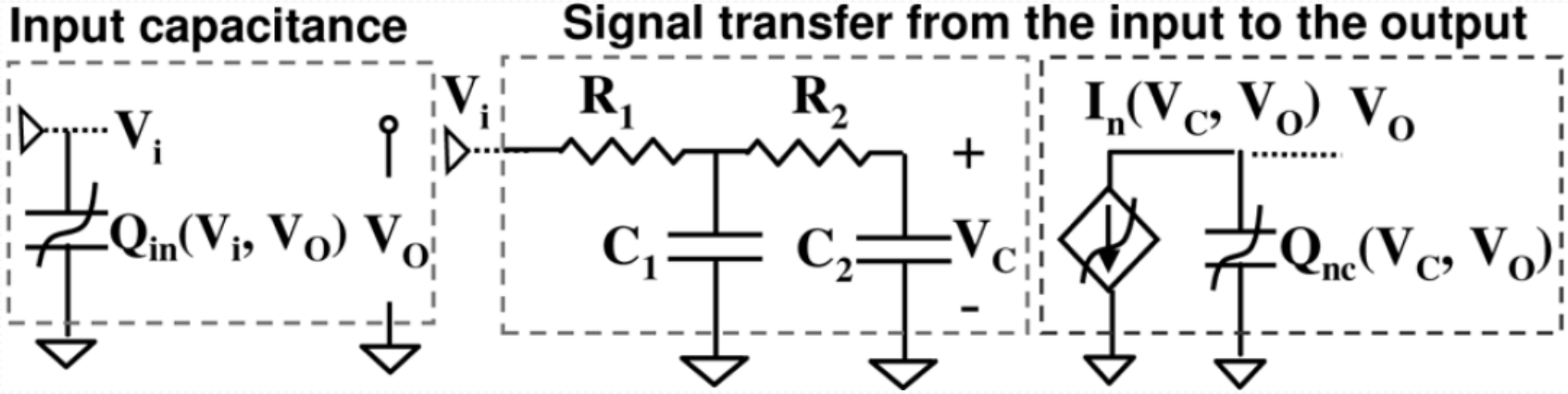
3. Waveform independent Model (WiM)

3.4 Detailed Model extraction Steps

Creation of the DC Current Look-up Table (LUT)

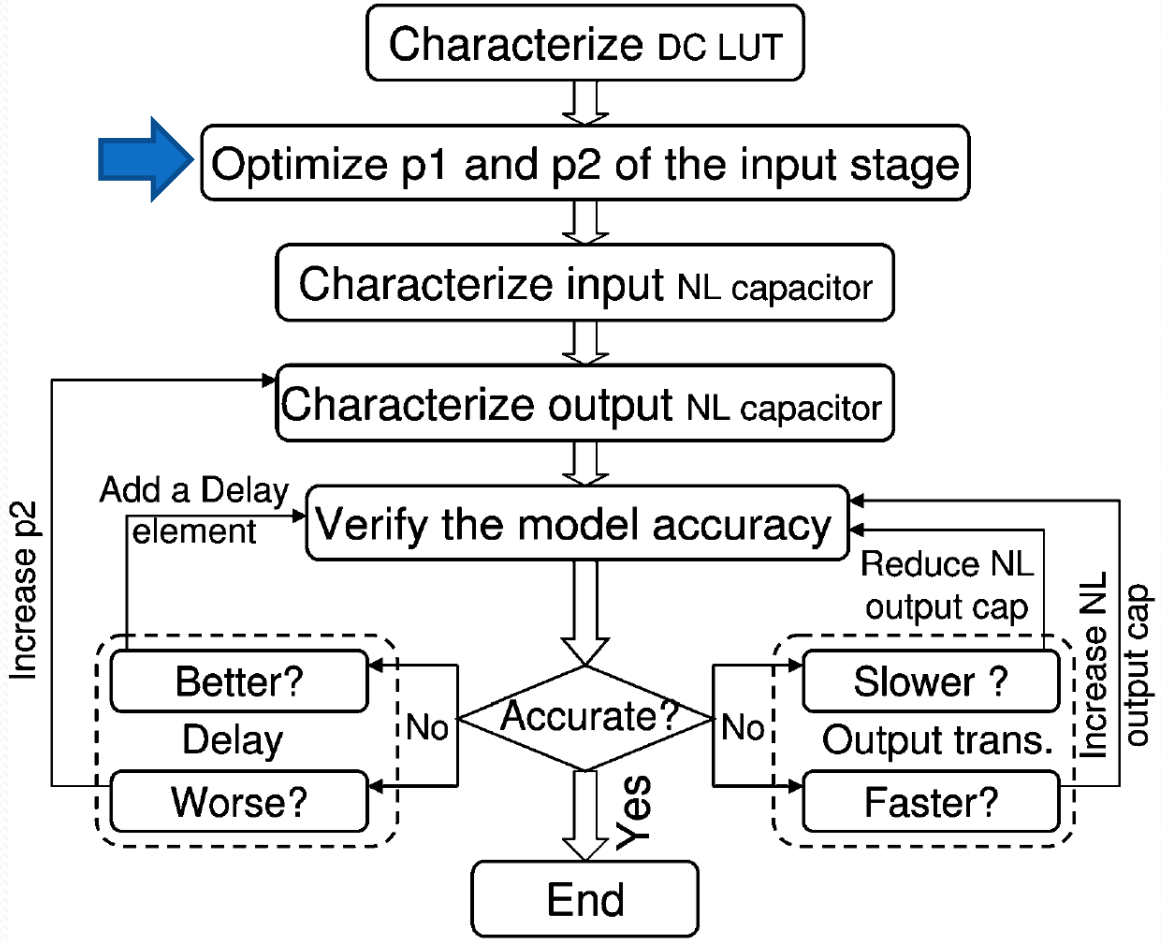
DC-voltage-level → no current in the nonlinear capacitances

➔ Current is exactly the current of the nonlinear current source



3. Waveform independent Model (WiM)

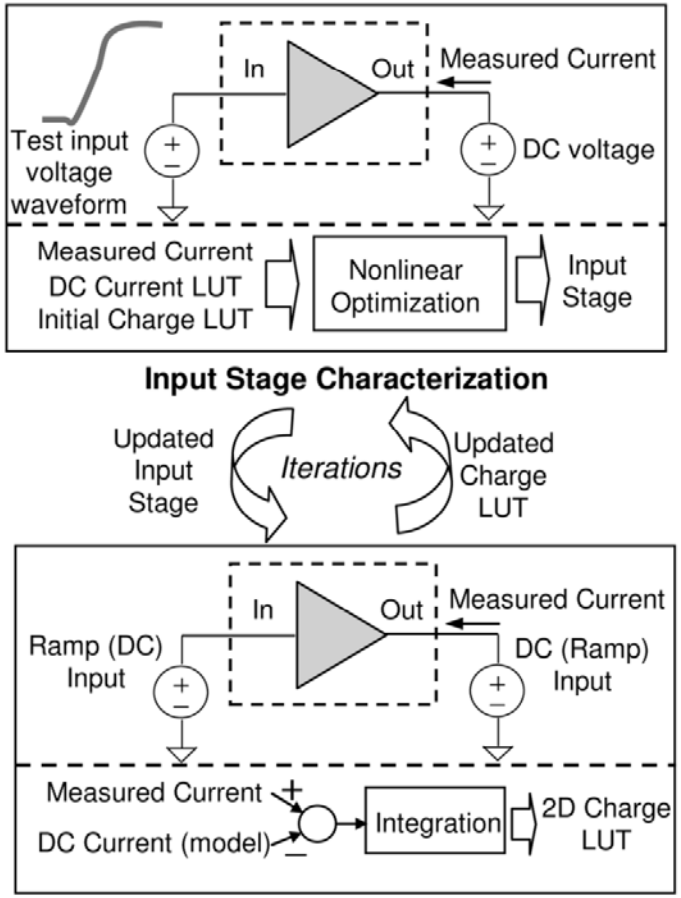
3.4 Detailed Model extraction Steps



3. Waveform independent Model (WiM)

3.4 Detailed Model extraction Steps

Extraction of the Input Stage (RC-stage)



- output voltage is fixed at a dc level
- transient input Voltage is applied
- nonlinear optimization to find

the optimal input RC parameters

in this process the nonlinear input charge is neglected

3. Waveform independent Model (WiM)

3.4 Detailed Model extraction Steps

Extraction of the Input Stage (RC-stage)

As the output is hold to a DC-voltage the nonlinear capacitance can be neglected

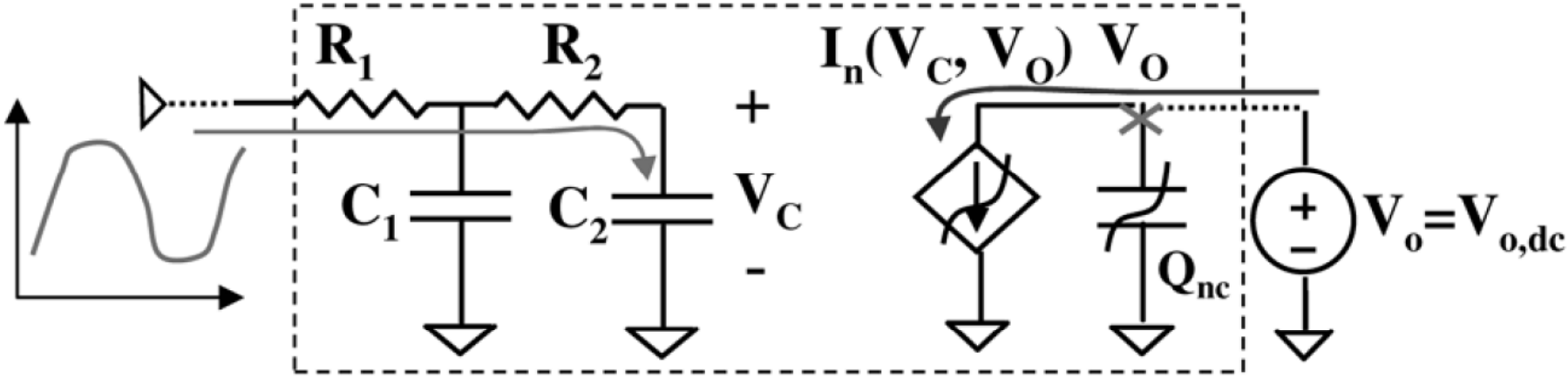
The input has a time-varying signal

➔ $I(V_o, t_i) = I_n(V_c(t_i), V_{o,\mathrm{dc}})$

$$H(s) = H_1(s) + H_2(s)$$

$$H_1(s) = \frac{k_1}{s + p_1}$$

$$H_2(s) = \frac{k_2}{s + p_2}.$$



3. Waveform independent Model (WiM)

3.4 Detailed Model extraction Steps

Extraction of the Input Stage (RC-stage)

➔we can calculate the error:

$$E(p_1, p_2, i) = \left(I(V_o, t_i) - I_n(V_c(t_i), V_{o,\mathrm{dc}})\right)^2 .$$

Utilization of least square fitting:

Condition of the minimum is:

$$\frac{\partial R^2}{\partial a} = 0$$

R: sum of the squares of the vertical deviations

a: variable

3. Waveform independent Model (WiM)

3.4 Detailed Model extraction Steps

Transfer function of one RC-stage

$$H_1(s) = \frac{Y(s)}{U(s)} = \frac{k_1}{s + p_1}$$

Usage of a Ramp: $u(t) = at$ ➔ $U(s) = \frac{a}{s^2}$

$$Y(s) = \frac{a}{s^2}\frac{k_1}{s + p_1} \rightarrow y(t) = ak_1\left(-\frac{1}{{p_1}^2} + \frac{t}{p_1} + \frac{1}{{p_1}^2}e^{-p_1 t}\right)$$

Same for $H_2(s)$ ➔ we get $V_c(t)$

3. Waveform independent Model (WiM)

3.4 Detailed Model extraction Steps

We differentiate $V_c(t)$:

$$\frac{\partial V_c(t)}{\partial t} = \frac{\partial y_1(t)}{\partial t} + \frac{\partial y_2(t)}{\partial t}$$

We differentiate our error function by the two parameters p_1 and p_2:

$$\frac{\partial E(p_1, p_2, t)}{\partial p_1} = -2(I(V_o, t_i) - I_n(V_c(t_i)) \cdot \frac{\partial I_n(V_c(t_i), V_{o,dc})}{\partial V_c(t_i)} \cdot \frac{\partial V_c(t_i)}{\partial p_1}$$

Condition for the Minimum $\frac{\partial E(p_1, p_2, t)}{\partial p_{1,2}} = 0$

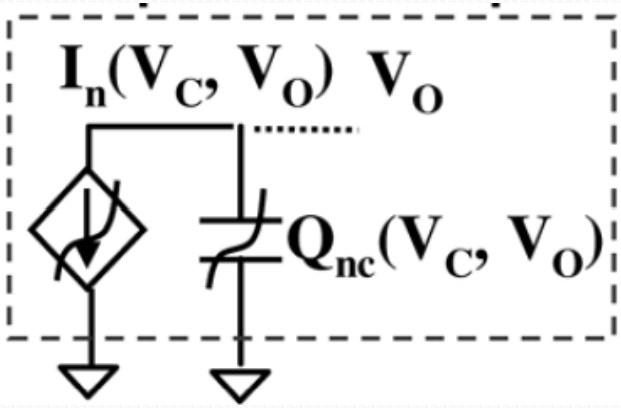
3. Waveform independent Model (WiM)

3.4 Detailed Model extraction Steps

Two variables and two equations ➔ done.

But the nonlinear output capacitor depends also on V_c

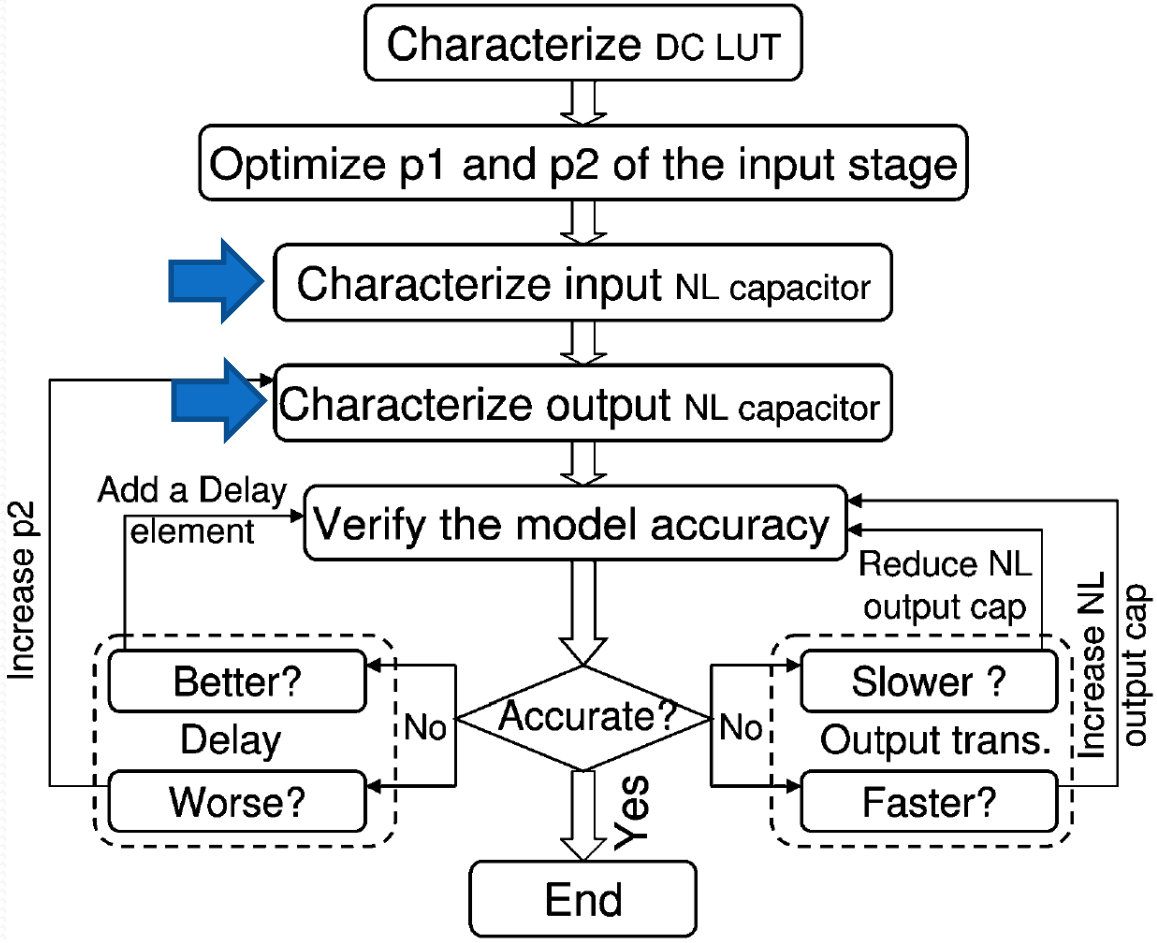
So it's not perfect



➔we have to redo the process for a near perfect estimation

3. Waveform independent Model (WiM)

3.4 Detailed Model extraction Steps



3. Waveform independent Model (WiM)

3.4 Detailed Model extraction Steps

Determination of the nonlinear charge LUT

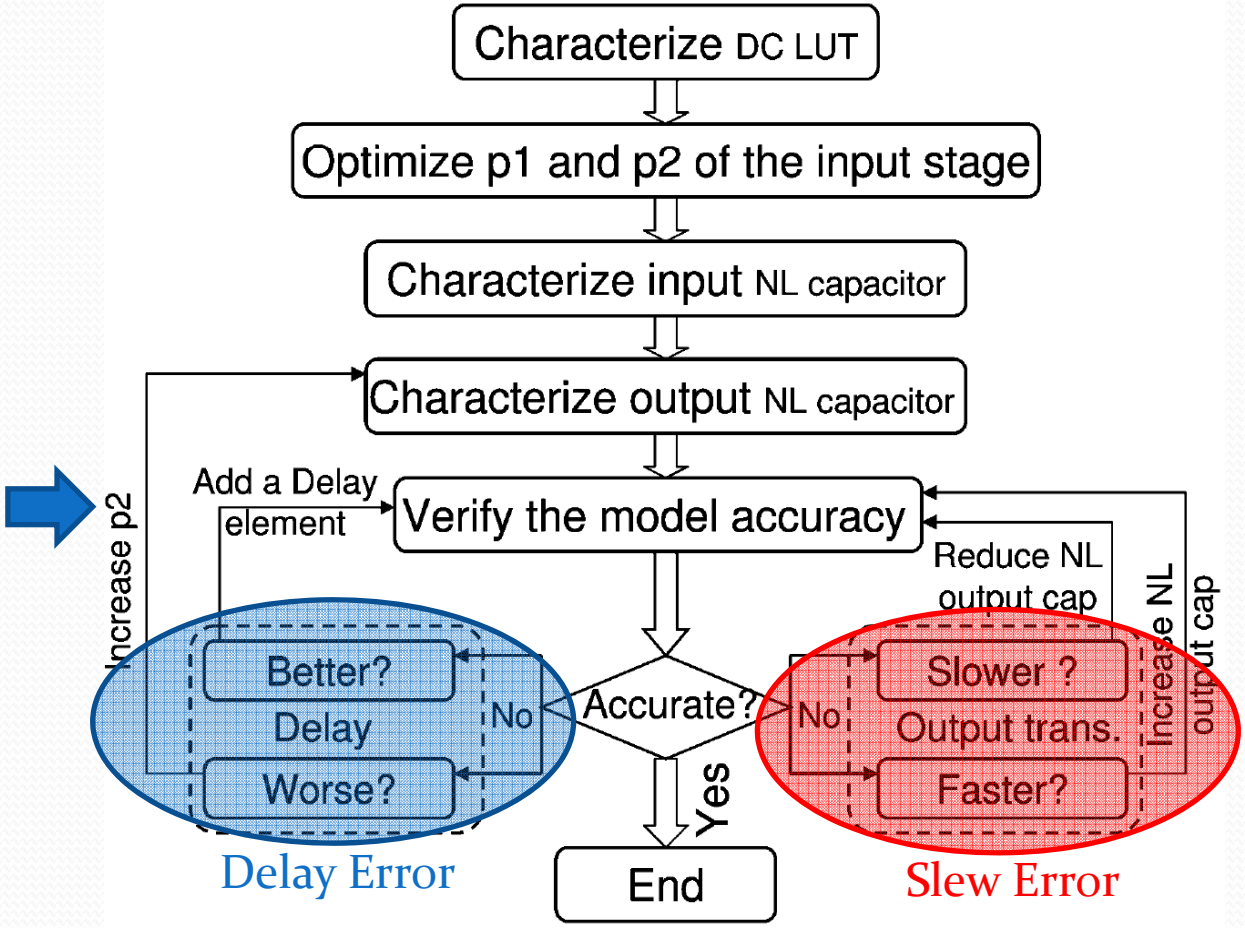
- o voltage input and ramp voltage output
- o voltage output and ramp voltage input

➔ Integral over the current gives nonlinear charge

- ➔ Current LUT is known → difference gives current
- ➔ RC-Stage is known → difference gives current

3. Waveform independent Model (WiM)

3.4 Detailed Model extraction Steps



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4. Parametrizable Waveform Independent Model

Idea:

- Addition of Process Voltage Temperature
- Adoption of the WiM-Model by combining response surface modeling technique (statistical reduction of the problem dimension)

➔Operating Temperature, threshold voltages, effective channel length, gate oxide thickness…
can be considered

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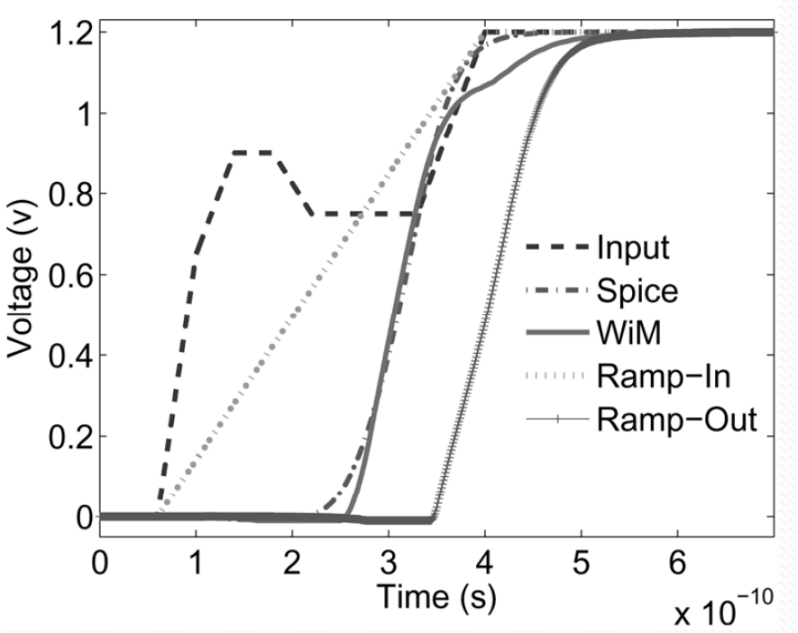
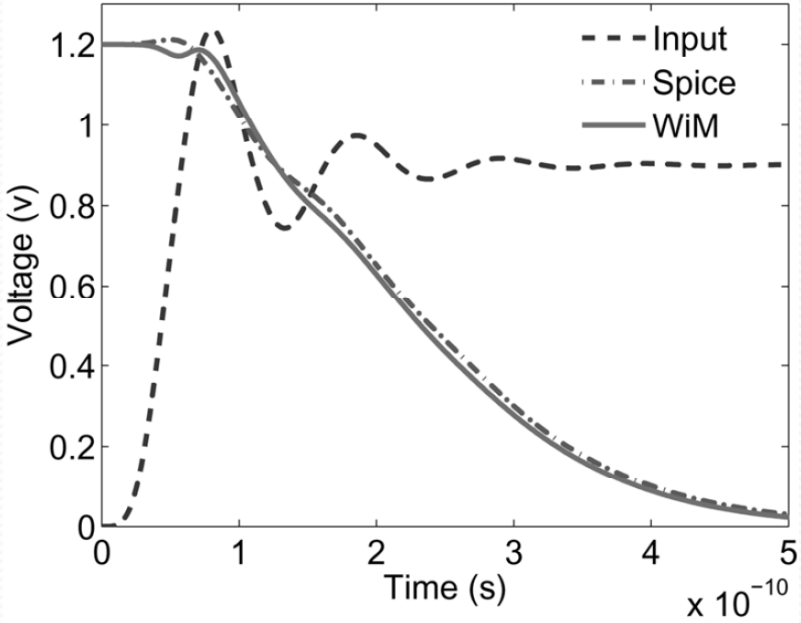
5. Experimental Results

5.1 Results using complex inputs



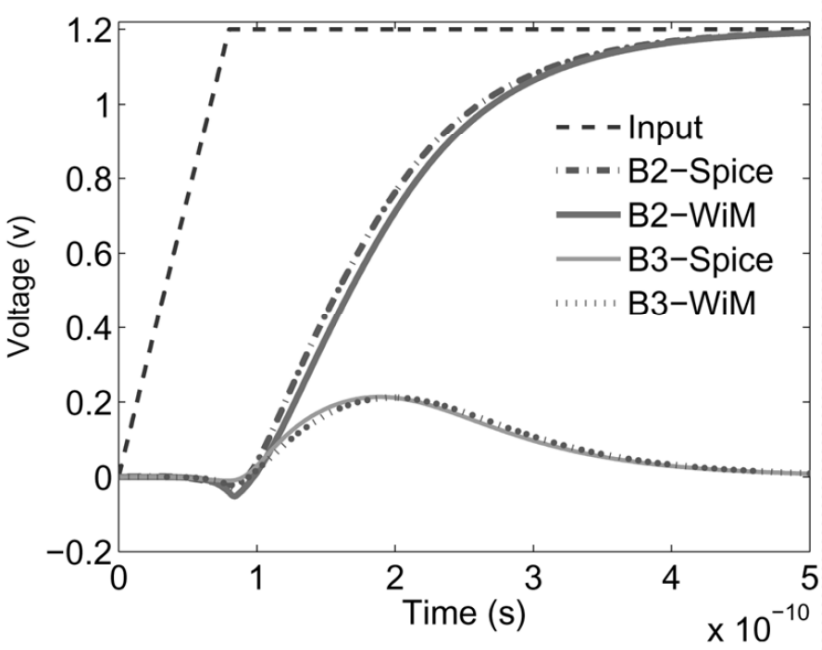
Three input OR driven by a complex input
In comparison with a ramp



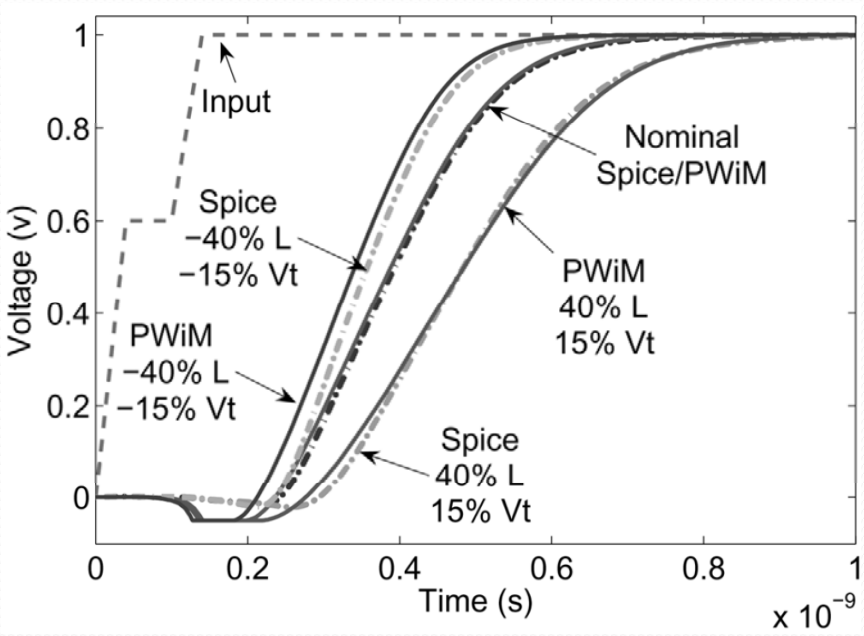
XOR gate driven by a complex input

5. Experimental Results

5.2 Results of Crosstalk Noise / Variational Modeling



Crosstalk analysis
Four-bit driven bus driven by buffers



Variational Modeling OR
L: channel length
Vt: Threshold voltage

5. Experimental Results

5.3 Delay / Slew Errors of WiM and the Speedup

- ➔ Maximum Error of 7.61% for Delay Noise
- ➔ Maximum Error of 5.27% for Slew Error
- ➔ Speedup up to 224 times over SPICE

Design	Input 1		Input 2		Speedup
	D. Err	S. Err.	D. Err	S. Err	
INVX1	0.08%	0.22%	0.21%	0.22%	83
INVX4	0.53%	0.92%	1.06%	0.26%	104
BUF2X1	1.71%	0.61%	0.49%	0.94%	128
BUF2X4	4.30%	1.55%	1.84%	2.48%	120
BUF4	4.80%	0.75%	4.77%	0.75%	179
AND2X1	3.20%	0.60%	2.21%	0.60%	98
AND2X4	5.13%	1.91%	3.75%	1.84%	115
AND2X8	6.55%	4.10%	4.78%	3.81%	151
AND3X1	2.87%	0.79%	2.83%	1.11%	158
AND3X4	5.27%	1.31%	5.17%	2.18%	104
AND4X1	2.04%	0.82%	1.97%	1.14%	147
AND4X4	3.95%	1.28%	3.83%	1.24%	188
NAND2X1	0.99%	1.03%	0.44%	0.64%	115
NAND2X4	1.71%	1.74%	0.70%	2.04%	118
NAND4X1	2.55%	1.08%	1.56%	1.09%	198
NAND4X4	4.23%	1.43%	2.75%	1.40%	224
AOI2X1	0.97%	3.05%	1.39%	3.04%	188
AOI2X2	0.32%	5.15%	0.97%	4.53%	136
OR3X1	4.92%	0.53%	4.32%	0.54%	182
OR3X4	7.61%	5.28%	6.63%	5.27%	173
XOR2X1	1.87%	0.09%	1.18%	0.12%	141
XOR2X4	4.81%	2.12%	3.68%	0.45%	214

5. Experimental Results

5.3 Delay / Slew Errors of WiM and the Speedup

Variational Modeling

➔ Maximum Error of 8.0% for Delay Noise
➔ Maximum Error of 11.1% for Slew Error
➔ Speedup up to 357 times over SPICE

Design	Delay %			Slew %			R.S.
	Var	Ave	Max	Var	Ave	Max	
INVX1	58	4.1	11	96	4.7	12.7	260
BUF2X4	78	7.3	17	132	6.5	17	357
BUF4	80	8.0	19	104	0.02	13.7	280
AOI2X2	129	7.4	34.2	192	11.1	33.6	357
OR3X4	87	5.4	16.8	132	5.8	16.9	259

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6. Conclusion

Advantages:

- Easy to adopt
- Near SPICE accuracy even for complex signals (5%)
- Uncoupled design can model multistage nonlinear drives
- Compactness of model libraries and the analysis efficiency
- Delay noise simulable
- 2nd Order of Magnitude speedup onto SPICE

Drawbacks:

- Multiple SPICE analysis are necessary

Discussion

- Is it a good idea to modelize the transistor with a current source?
- Should we use a two stage model?
- Is it a good idea to use nonlinear devices?
- Is it combinable with statistical analysis?
- Fullfills the model our requirements?