Extended Applications of Current Source Modeling

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I. Introduction

As described in [1], feature sizes are getting smaller due to the decrease of layout geometries to less than 65 nm, which results in an increased packing density and frequency. Since the interconnect is getting longer, the impact of analog effects there are increasing, too. These effects, the most important of them being the capacitive crosstalk noise, are considered noise and have to be modeled in order to be able to do an accurate timing analysis.

The capacitive crosstalk noise, for example, results from the interference of the interconnects between logic cells. If the waveform in one interconnect changes, this influences the other interconnects next to it, modifying waveform and delay.

However, not only the crosstalk noise alters the delay of a cell, but it is also dependent on the waveform of the input voltage, since a different input voltage waveform causes a different delay. Therefore there is a need for a current source model, which is load independent and which can handle an arbitrary input waveform.

The base for each current source model is the basic NMOS/PMOS transistor model as shown in Fig. 1. Depending on which logic cell has to be modeled, the transistors are connected and the resulting circuit is simplified by combining some parts and omitting others, resulting in the current source model.

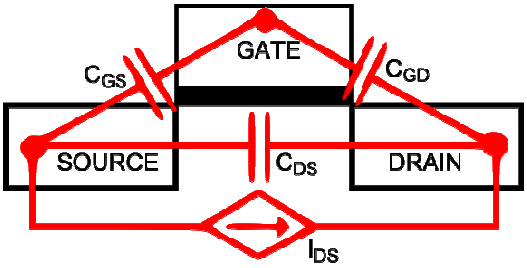


Fig. 1: Model for a NMOS/PMOS Transistor

The first model that could deal with an arbitrary input and output voltage waveform and any load, was Blade and its corresponding interconnect model Razor, which is the algorithm used to calculate the output waveform. This model, as introduced in [2], uses an internal capacitance and a voltage controlled current source, connected as shown in Fig. 2. There is also an input waveform time shift, which is needed to adapt to the delay of the cell, since the current source and the capacitance only produce the right waveform but not the right delay. Since Blade is a rather simple model, it only has a limited accuracy, also because the necessary time shift is difficult to determine. That is one of the reasons why the authors of [1] introduced another current source model for combinatorial cells.

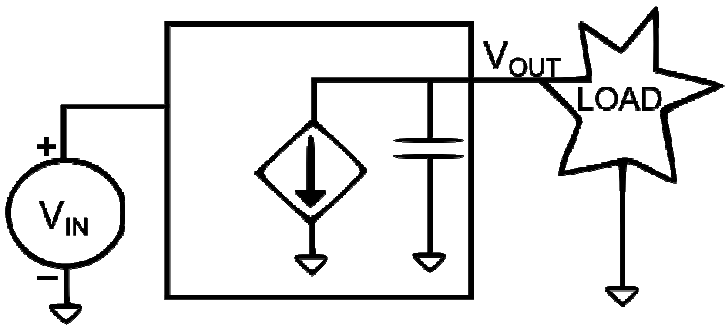


Fig. 2: The Blade Current Source Model

II. Combinational Model

A combinatorial logic cell is a CMOS logic cell, in which the output voltage depends only on the input voltage, i.e. there are no feedback loops. For this kind of logic cell, the combinatorial current source model, as introduced in [1], is able to calculate the output voltage to an arbitrary input voltage with a result that is almost as accurate as SPICE. The main difference between this model and the existing ones is that this model tries to capture parasitic effects between the input and the output node. In this section, the derivation of the size of the components in the model will be shown with the help of an inverter and a transmission gate.

II.1 Inverter

This current source model basically consists of 3 capacitances and one voltage controlled current source connected as shown in Fig. 3. The capacitance C_M, that connects the input and the output node, is called Miller capacitance and this is where this model differs from previous ones, since this capacitance captures parasitic effects between these two nodes.

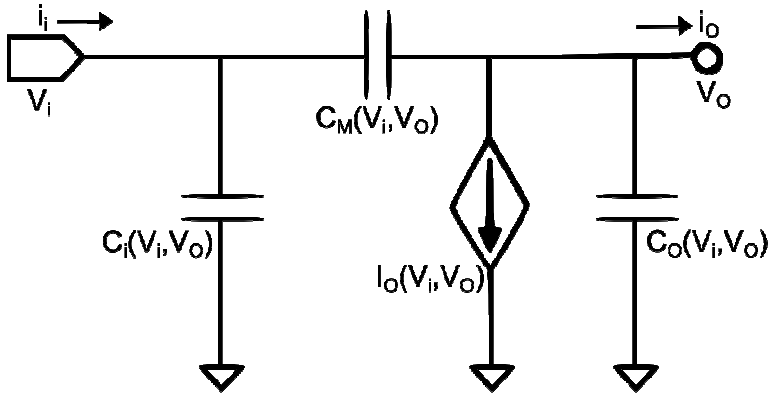


Fig. 3: Current source model for a combinatorial logic cell

Before this model can be used, the sizes of the elements need to be determined. In order to do this, some equations have to be established. The two equations are derived by means of the Kirchhoff Current Law at the two nodes, input and output node.

At the output, there are four current contributors: the two currents through the capacitances, the output current and the one from the current source. Since the Miller capacitance connects the input and the output, a change in either of the two voltages leads to a current flowing through the node. This is why there are two entries, containing C_M, in the equation.

$$i_O + I_O(V_i, V_O) + \left(C_O(V_i, V_O) + C_M(V_i, V_O)\right)\frac{dV_O}{dt} - C_M(V_i, V_O)\frac{dV_i}{dt} = 0 \qquad (1)$$

An equal equation can be derived for the input node, for which the two current through the input capacitance and through the Miller capacitance have to be considered in addition to the input current.

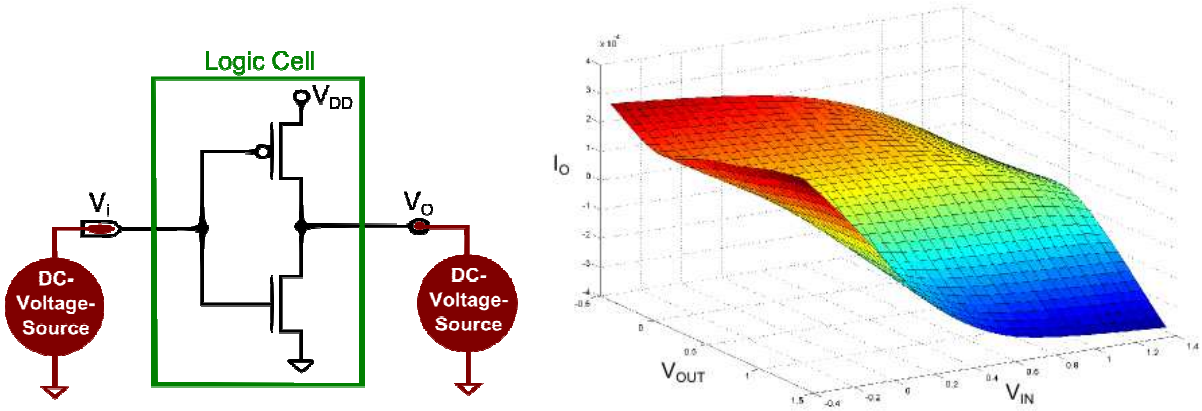
$$i_i + \left(C_i(V_i, V_O) + C_M(V_i, V_O)\right)\frac{dV_i}{dt} - C_M(V_i, V_O)\frac{dV_O}{dt} = 0 \qquad (2)$$

These two equations are the base for the characterization of the elements of the current source model.

The first element that can be determined is the current, flowing through the current source. Since its value depends on both the input and the output voltage, a table has to be established, in which the values of the current are put down at different voltage levels. Therefore, two DC-voltage-sources are connected to the logic cell as shown in Fig. 4(a). Without the voltage changing over time the derivatives in equation (1) become zero and the equation simplifies.

$$i_O + I_O(V_i, V_O) = 0 \tag{3}$$

The DC-voltage sources are swept from $-\Delta$ to $V_{DD}+\Delta$. The authors of [1] use 33 steps for each voltage source leaving them with a 33x33 table for the current through the current source. This current can be determined by measuring the output current, since equation (3) shows that the current through the current source is simply the negative output current. The approximate values of the current, plotted over the input and the output voltage, can be seen in Fig. 4(b).



(a) (b)

Fig. 4: (a) Arrangement for determination of the values of I_O, (b) Plot of the values over V_{IN} and V_{OUT}

The next element of which the values can be determined subject to the input and output voltages is the Miller capacitance. If a DC-voltage-source, which is swept from $-\Delta$ to $V_{DD}+\Delta$, is connected to the output node and a saturated ramp voltage to the input node, equation (1) simplifies to equation (4) which can be solved for the Miller capacitance.

$$i_O + I_O(V_i, V_O) - C_M(V_i, V_O)\frac{dV_i}{dt} = 0 \tag{4}$$

With the values of the current source already determined in the first step and a known slope of the saturated ramp, the values for the Miller capacitance can be calculated, using equation (4). To get more accurate values for C_M, the authors of [1] do the characterization several times, each time with a different slope of the ramp and then use an average value for the table. This does not make such a big difference, though, since a change in the slope also changes the measured output current and these differences almost cancel out.

With the current source and the Miller capacitance already characterized, only two unknown capacitances are left. The determination of their values is rather similar to the characterization of the Miller capacitance.

For the determination of the input capacitance, the voltage sources are connected exactly the same as for the characterization of the Miller capacitance, a DC-voltage-source (swept from $-\Delta$ to $V_{DD}+\Delta$) connected to the output node and a saturated ramp to the input node. In this case, equation (2) simplifies to a form, containing the input capacitance as the only unknown.

$$i_i + \left(C_i(V_i, V_O) + C_M(V_i, V_O)\right)\frac{dV_i}{dt} = 0 \quad (5)$$

This equation can be solved for the input capacitance and if the value of the input current is measured for the different voltage levels and slopes, the values for C_i can be put down in yet another table.

To determine the values for the output capacitance, the input node is connected to a DC-voltage-source and the output node to a saturated ramp. In this case, equation (1) simplifies to a form, which contains C_O as the only unknown.

$$i_O + I_O(V_i, V_O) + \left(C_O(V_i, V_O) + C_M(V_i, V_O)\right)\frac{dV_O}{dt} = 0 \quad (6)$$

Since the values for the Miller capacitance, the current source and the slope are already known, the values of the output capacitance can be calculated if the output current is measured.

With all parameter determined as a function of input and output voltage, equation (1) is a differential equation, that can be solved for the output voltage, when any input voltage is connected to the input node, when an arbitrary load is connected to the output node and when the output current is a function of the output voltage and the load. This differential equation can be solved to determine the output voltage using e.g. Euler's method.

This model works for all logic cells with only one input and one output. If a logic cell has more than one input, the model looks a bit different as the current source model for the transmission gate will show.

II.2 Transmission Gate

A transmission gate as shown in Fig. 5(a) consists of an NMOS and a PMOS transistor that are connected in parallel, so the current flowing through it depends on four voltages: the two voltages at the gates, input and output voltage. This dependence on four variables makes the tables for the elements of the current source rather big since they will have to be 4-dimensional, but this problem will be dealt with later in this section. There are three cases in which the transmission gate can work: off, conducting and in rising or falling transition. If it is off, there will be no connection between input and output node. In the case when it is conducting, the input voltage equals the output voltage and in transition, any voltage between high level and low level is possible.

The current source model for the transmission gate can be derived from the form shown in Fig. 5(b). This would already be a current source model, but to make it easier to handle, the current source connecting input and output node is divided into two current sources connected to ground as shown in Fig. 5(c).

As mentioned before, most of the components depend on all four input voltages, which results in 4-dimensional tables that need a lot of memory capacitance. To reduce that effort, all the components can be divided into two parts, both depending on input and output voltage, one part also depending on the clk-voltage and the other one on the clk_bar-voltage. For example, the input current source can then be written as shown in equation (7).

$$I_{IN} = I_{IN-CLK}(V_{IN}, V_{OUT}, V_{CLK}) + I_{IN-CLK\_bar}\left(V_{IN}, V_{OUT}, V_{CLK\_bar}\right) \quad (7)$$

The output current source and the capacitance can also be split that way, except C_{CLK} and C_{CLK_bar}, which already depend only on V_{IN}, V_{OUT}, V_{CLK} and V_{IN}, V_{OUT}, V_{CLK_bar}, respectively. For further information, please refer to [1].

These basic current source models can be used to derive the sequential model that will be discussed in the following section.

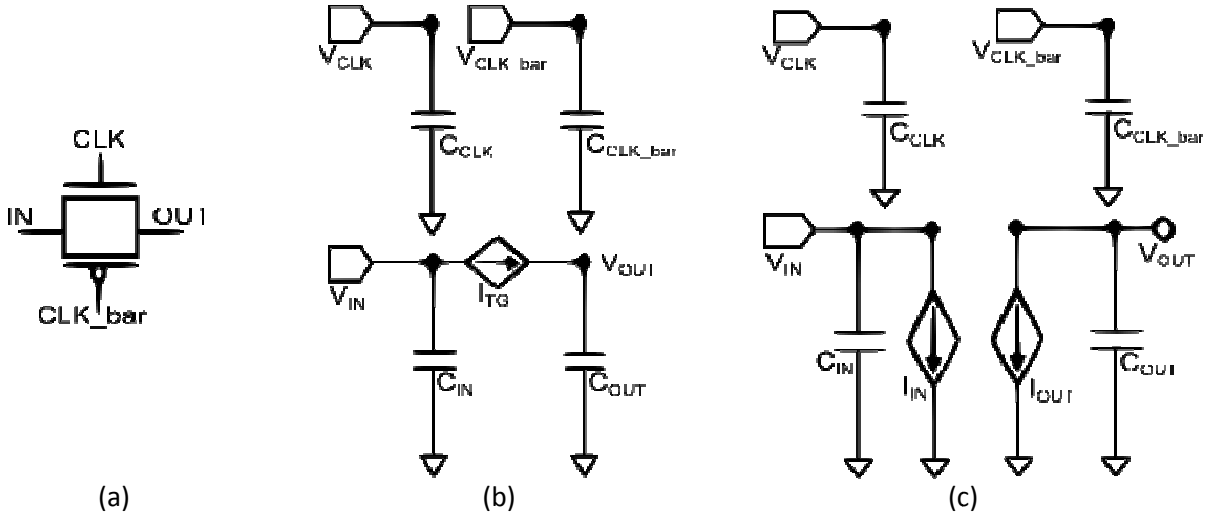


Fig. 5: (a) Transmission Gate, (b) current source model, (c) decoupled current source model

III. Sequential Model (CMOS Latch)

The difficulty with sequential logic cells is that noise can be magnified because of the feedback loops, since here, input and output are mutually dependent. The authors of [1] were the first to derive a current source model for sequential cells. In the following this will be illustrated with the help of a CMOS latch shown in Fig. 6.

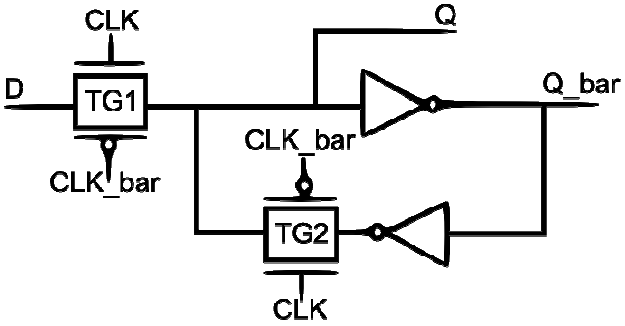
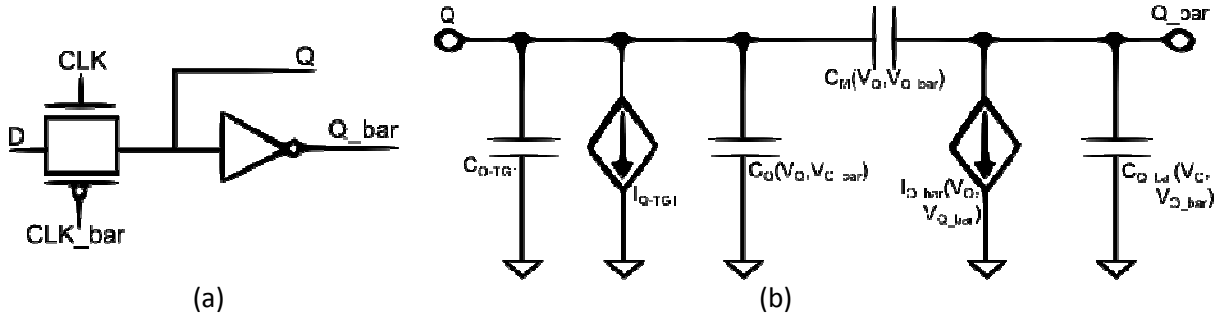


Fig. 6: CMOS Latch

This latch can be in three different modes, depending on the transmission gates being either conducting, off or in transition.

The case, when CLK is high, the first transmission gate conducting and the second one off, is called Transparent Mode. Since the transmission gate in the feedback loop is off, there is no connection in the feedback loop, which is displayed in Fig. 7(a), and the output Q is equal to the input D.

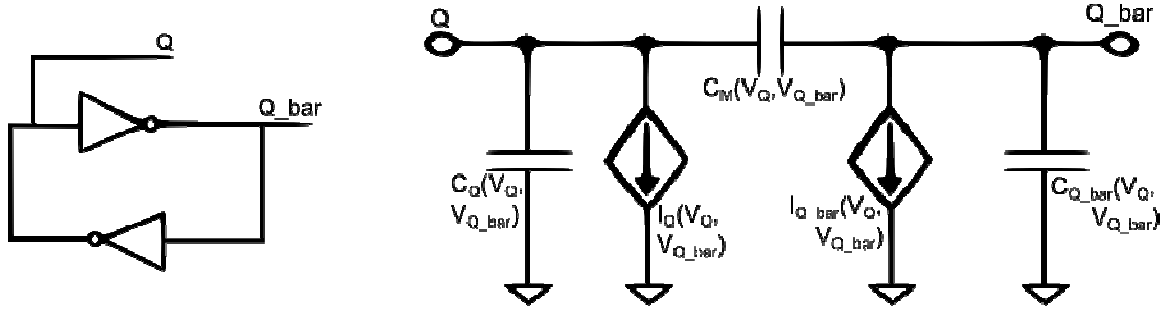
The current source model can be derived easily by connecting the output node of the model for a transmission gate to the input node of an inverter model, resulting in a connection between Q and Q_bar modeled as shown in Fig. 7(b), a current source model with four capacitances and two voltage controlled current sources. The three input nodes CLK, CLK_bar and D, which are connected to a capacitance (CLK and CLK_bar) or a capacitance and a current source (D), are also part of the model.



(a) (b)

Fig.7: (a) Latch in Transparent Mode, (b) Current Source Model for Latch in Transparent Mode

Opaque Mode is the mode, when CLK is low, the transmission gate in the feedback loop is conducting and the one connected to D is off. Here, the input data D is disconnected and Q and Q_bar stabilize each other, which can be seen in Fig. 8(a). The current source model can be derived easily by connecting the input node of an inverter model the output of another one and vice versa. The simplification of this leads to the model in Fig. 8(b).



(a) (b)

Fig. 8: (a) Latch in Opaque Mode, (b) Current Source Model for Latch in Opaque Mode

The third mode is called Transition Mode and occurs, when CLK is in transition, so there is either a falling or a rising slope. In this case, all components of the latch have to be considered, since all of them influence the output. This results in the current source model for Transition Mode being the same as for the complete model.

The current source model for the complete latch can be derived by combining the models for Opaque Mode and Transparent mode and adjusting them. The result is shown Fig. 9.

The characterization for the latch is more complex than the characterization of the inverter model but it is done similarly. Again, Kirchhoff's Current Law is used to derive three equations for the currents flowing through the nodes next to Q_bar (8), Q (9) and D (10).

$$i_{L-Q\_bar} + I_{Q\_bar}(V_Q, V_{Q\_bar}) - C_M(V_Q, V_{Q\_bar})\frac{dV_Q}{dt} + \left[C_M(V_Q, V_{Q\_bar}) + C_{Q\_bar}(V_Q, V_{Q\_bar})\right]\frac{dV_{Q\_bar}}{dt} = 0 \quad (8)$$

$$i_{L-Q} + I_Q + i_{Q-TG1} - C_M(V_Q, V_{Q\_bar})\frac{dV_{Q\_bar}}{dt} + \left[C_M(V_Q, V_{Q\_bar}) + C_Q + C_{Q-TG1}\right]\frac{dV_Q}{dt} = 0 \quad (9)$$

$$i_D + I_{D-TG1} + C_{D-TG1}\frac{dV_D}{dt} = 0 \quad (10)$$

Characterization starts with Transmission Gate 1. Then all the other capacitances and currents in the three modes can be determined by alternately attaching dc-voltage sources and ramp voltages to the input and the output nodes and putting the measured data down in tables. A detailed description can be found in [1].

When all the values of the components have been determined, the output voltage can be determined by solving the differential equations (8) and (9).

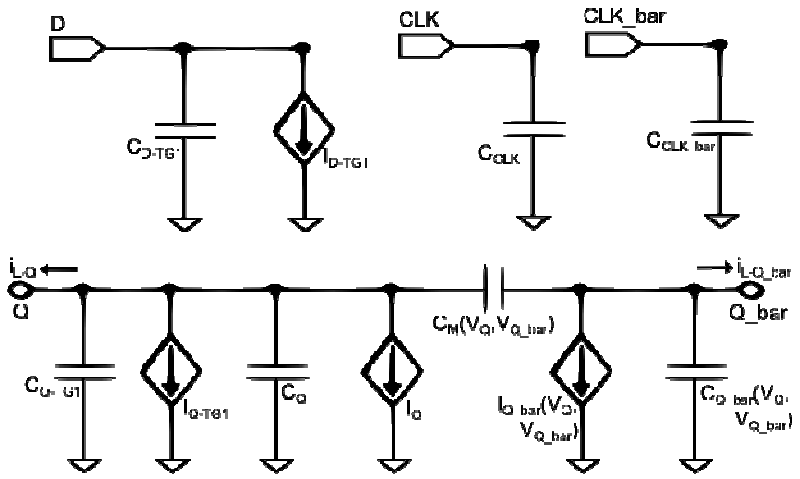


Fig. 9: Current Source Model for the complete CMOS latch

IV. Conclusion

The authors of [1] derived a new current source model for Combinatorial Logic Cells, which can be used to determine the output voltage waveform and through that the delay of the logic cell. They claim that the results were almost as accurate as SPICE.

This model made it also possible to derive a current source model for Sequential Logic Cells, modeling the noise amplification in feedback loops which had not been done before.

These models can be used to calculate the output voltage to an arbitrarily shaped input voltage and to any load attached to the output.

References

[1] S. Nazarian, H. Fatemi and M. Pedram, “Accurate Timing and Noise Analysis of Combinational and Sequential Logic Cells Using Current Source Modeling” in *IEEE Transactions on very Large Scale Integration (VSLI) Systems*, Vol. 19, No. 1, January 2011

[2] J. F. Croix and D. F. Wong, “Blade and Razor: Cell and interconnect delay analysis using current-based models” in *Proc. Des. Autom. Conf.*, 2003, pp. 386-389